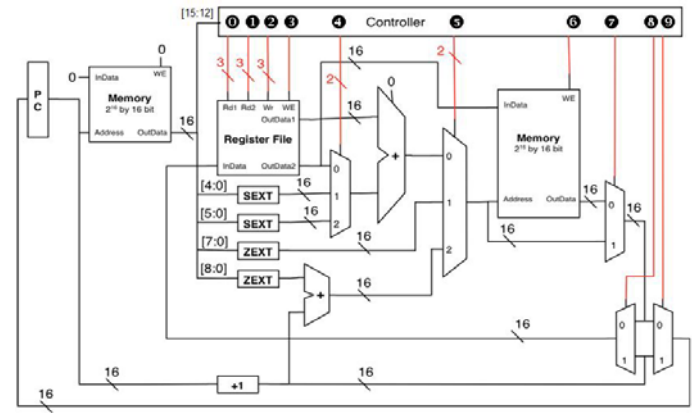


Datapath Breakdown

(Additional notes to Datapath)

CIT 595
Spring 2008

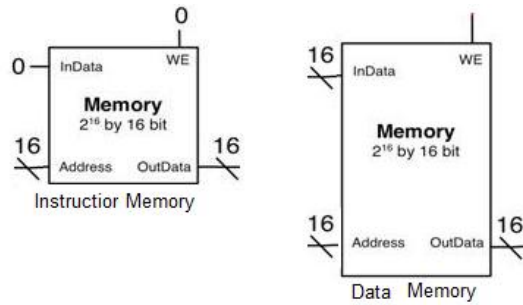
Data Path



CIT 595

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Memory

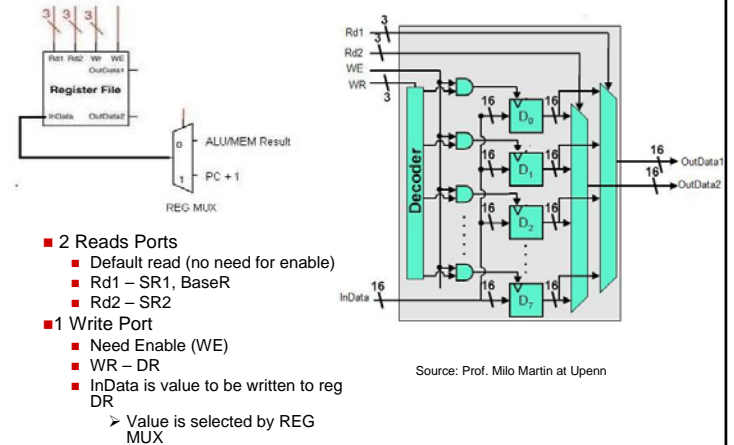


- Instruction Memory is default set to read
- Data Memory can be read or written based on WE
 - WE = 1 means write

CIT 595

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Registers/ Register File



- 2 Reads Ports
 - Default read (no need for enable)
 - Rd1 – SR1, BaseR
 - Rd2 – SR2
- 1 Write Port
 - Need Enable (WE)
 - WR – DR
 - InData is value to be written to reg DR
 - Value is selected by REG MUX

Source: Prof. Milo Martin at Upenn

CIT 595

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ALU

- ADD
 - Reg-Reg
 - Immediate
 - Bits [4:0]
 - Default control unit signal set to 0 for ADD
- LDR, STR
 - Used to evaluate the address of the load and store
 - Bits [5:0]
- Expand to accommodate NOT instruction

CIT 595 5

Memory Address MUX (for Data Memory)

CIT 595 6

PC and PC MUX

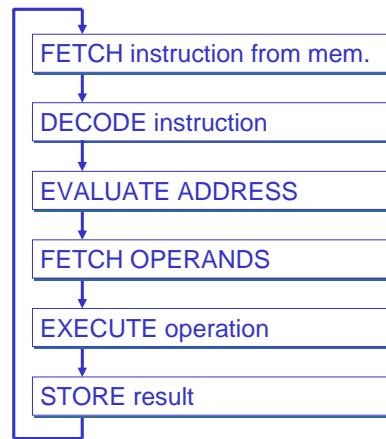
- PC (16-bit register) update is based on the PC MUX
 - PC + 1(default)
 - Address based on BR, JMP, TRAP
 - For BR to work in this implementation need CC registers

CIT 595 7

Control Unit

CIT 595 8

Instruction Cycle



CIT 595

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Instruction Cycle Variation

In the simple implementation

- Evaluate Address and Execute both use ALU, we can make this one phase

- The Operand Fetch is separated into Register Fetch and Memory Fetch

CIT 595

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