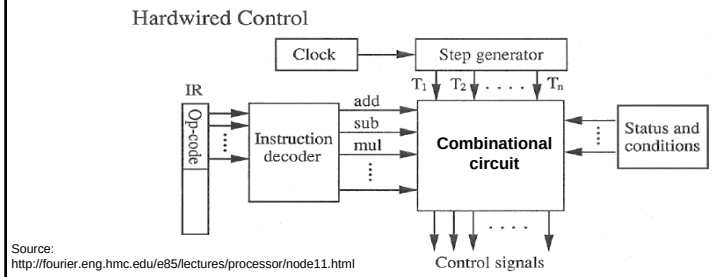
Hardwired Control

CIT 595
Spring 2008

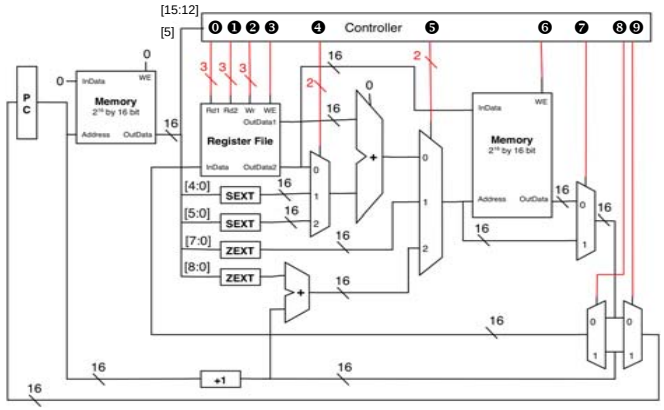
Hardwired Control



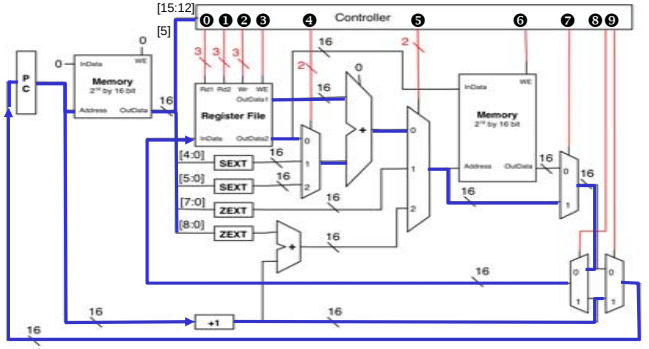
Source:
http://fourier.eng.hmc.edu/e85/lectures/processor/node11.html

- Control signals are combination of
  - Opcode bits
  - Other signals such as interrupts, or condition codes (NZP)
  - Timing info (T1 to Tn) – these signals are essential for timing for proper sequencing through instruction cycle

Hardwired Implementation of LC3

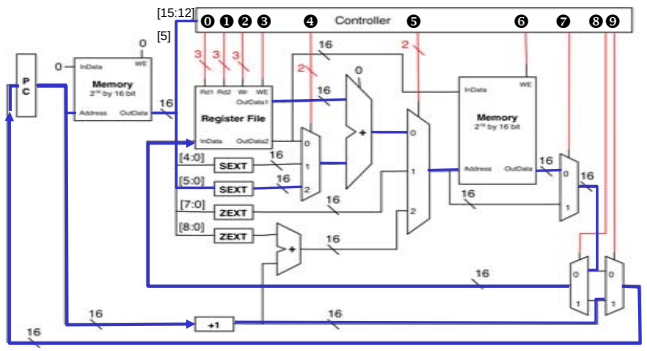


ADD Instruction



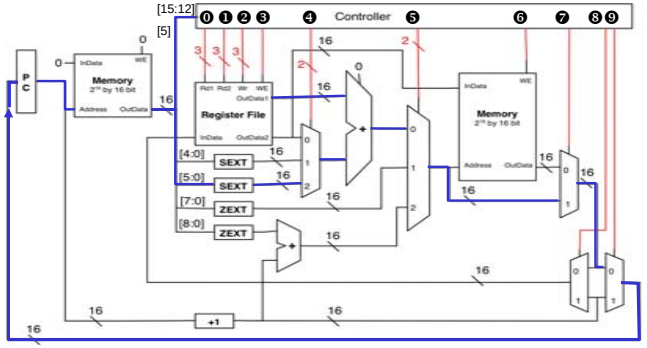
	Opcode		Control									
Instr	I[15:12]	I[5]	❶	❷	❸	❹	❺	❻	❼	❽	❾	❿
ADD	0001	0	I[8:6]	I[2:0]	I[11:9]	1	00	00	0	1	0	1
			SR1	SR2	DR							

LDR Instruction



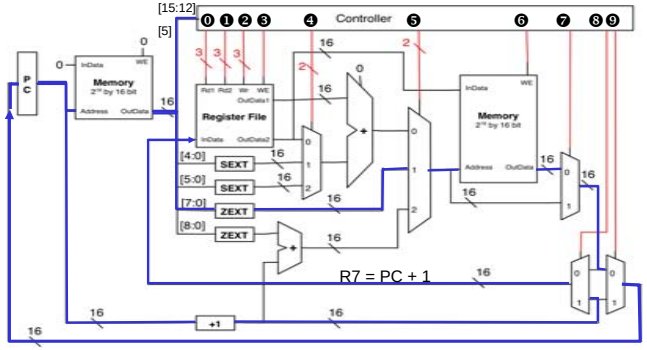
	Opcode		Control									
Instr	I[15:12]	I[5]										
LDR	0110	-	I[8:6]	-	I[11:9]	1	10	00	0	0	0	1
			BaseR		DR							

JMP Instruction



	Opcode		Control									
Instr	I[15:12]	I[5]										
JMP	1100	-	I[8:6]	-	-	0	10	00	0	1	x	0

TRAP Instruction



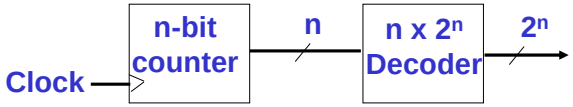
	Opcode		Control									
Instr	I[15:12]	I[5]										
TRAP	1111	-	-	-	111(R7)	1	xx	01	0	0	1	0

Sequencing of Instructions

- For appropriate sequencing i.e. F->D->EA->OP->EX->S
  - Updating PC and condition code registers
  - Reading/Updating Registers and Memory
- Use clock to sequence each phase of an instruction by raising the right signals as the right time
- It takes fixed number of clock ticks/cycles (repetition of rising or falling edge) to execute each instruction
- How is this done?

Sequencing the Stages in Hardwired Implementation

- We connect the clock to a synchronous counter and the counter to the decoder
- The decoder output enabled is based on counter outputs (i.e. which cycle you are in)
- The decoder output is then ANDed with the controls signals generated to enable only certain control signals during a particular cycle



Sequencing Instruction Stages in Hardwired Implementation (contd..)

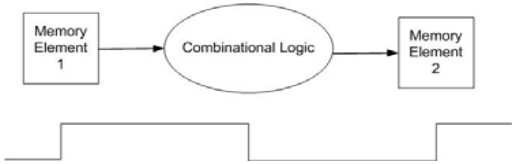
- Example:
  - Max. number of cycles an instruction takes is 6
    - Goes through F->D->EA->OP->EX->S
  - Then we would need 3-bit counter whose outputs are fed into 3 x 8 decoder
  - The output of the decoder, T_0 to T_7 are enable based on count i.e.
    - T_0 = 1 when count = 000, all others are disabled
    - T_5 = 1 when count = 101, all others are disabled
  - The decoder outputs are ANDed with control generated signals to produce the behavior required during each phase

Clocking Methodology

- How long should the clock cycle be such that we complete a one phase of the instruction cycle?
- When is data valid or stable?
  - So that it can be read or written
  - Do not want to end with mix of old and new data
- In a processor only *memory elements* can store values
- This means any collection of combinational logic must have its
  - Inputs coming from a set of memory elements and
  - Outputs written into a set of memory elements

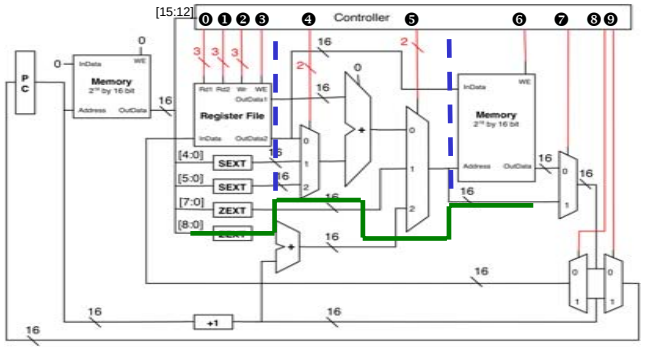
Clocking Methodology (contd..)

- The length of the clock cycle is determined as follows:



- The time necessary for the signals to reach memory element 2 defines the length of the clock cycle
  - i.e. minimum clock cycle time must be at least as great as the maximum propagation delay of the circuit

Example of Clock Cycle Length



Hardwired Control Implementation Adv & Disdav

- Fast (Advantage)
  - Once the instruction decoded, instruction bits are used to generate the control signals
- Static (Disadvantage)
  - Instruction and control logic are tied together, which makes it difficult to modify or add new instructions