

Milo M. K. Martin

Curriculum Vitae

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Computer and Information Sciences Department
University of Pennsylvania
3330 Walnut Street
Philadelphia, PA 19104-6389
U.S. Citizen

E-mail: milom@cis.upenn.edu
Web: www.cis.upenn.edu/~milom/
Office: (215) 746-2972
Fax: (215) 898-0587

Education

- **Ph.D. Computer Science**, December 2003
Computer Sciences Department, University of Wisconsin, Madison, WI, USA
- **M.S. Computer Science**, May 1998
Computer Sciences Department, University of Wisconsin, Madison, WI, USA
- **B.A. Honors Computer Science**, *magna cum laude*, May 1996
Gustavus Adolphus College, St. Peter, MN, USA

Employment

- January 2004-present, **Assistant Professor**
Dept. of Computer and Information Science, University of Pennsylvania, Philadelphia, PA, USA
- June 1997-December 2003, **Research Assistant**
Computer Sciences Department, University of Wisconsin, Madison, WI, USA
- June 1998-September 1998, **Intern**
IBM Server Development Group, Rochester, MN, USA
- August 1996-June 1997, **Teaching Assistant (Instructor)**
Computer Sciences Department, University of Wisconsin, Madison, WI, USA

Honors and Awards

- NSF's Faculty Early Career Development (CAREER) Award, FY 2007
- Two papers selected for IEEE Micro's Top Picks Issue (2003, 2006)
- Gustavus Adolphus College's *First Decade Outstanding Achievement Award*, 2006
- Norm Koo Fellowship from Sun Microsystems, 2002-2003 (One academic year)
- IBM Graduate Fellow, 1997-2002 (Five academic years)

Research Interests

My research interests include multiprocessor and multi-core memory systems, cache coherence protocols, transactional memory systems, shared-memory workloads, scalable processor micro-architectures, verification of concurrent hardware and software, hardware support for secure systems, and programming models for next-generation multi-core hardware architectures.

Grants

Pending

- NSF TC: *Medium: Ironclad: Securing Low-Level and Legacy Code against Memory Vulnerabilities*. PI with Co-PIs Steve Zdancewic and Amir Roth. \$1,200,000 (four years).

Awarded

- NSF CCF-SHF: *Medium: Formal Analysis of Concurrent Software on Relaxed Memory Models*, CCF-0905464. Co-PI with PI Rajeev Alur, \$1,200,000 (four years, 2009-2013). Program director: Sol Greenspan
- NSF *Multicore Bootcamp: REU Supplement*. PI. \$16,000 (one year, 2009).
- NSF CPA-CSA: *BLUE CHIP: Security Defenses for Misbehaving Hardware*, CCF-0810947. Co-PI with PI Jonathan Smith, \$200,000 (three years, 2008-2010). This award is Penn's half of a joint project with Sam King at University of Illinois. Program director: Chitaranjan Das
- DARPA *Terabit Edge Research Activity* Co-PI with PI Jonathan Smith, Department of the Air Force, Sponsor # FA8650-07-C-7743, \$270,843 (one year, 2007-2008).
- NSF CAREER: *Semantics and Hardware Implementation of Transactional Memory*, CCF-0644197. PI, \$400,000 (five years, 2007-2011). Program director: Almadena Chtchelkanova
- NSF ON-Core: *Single-thread Performance via Multi-core Aggregation*, CCF-0541292 Co-PI with PI Amir Roth, \$400,000 (three years, 2006-2009). Program director: Timothy Pinkston
- Intel Research Grant: *Hardware Support for Memory-Safe C*. PI, \$120,000 (three years, 2007-2010). Intel technical contact: Joel Emer
- Intel Research Grant: *Toward Simpler Multiprocessor Designs*. PI, \$120,000 (three years, 2004-2007). Intel technical contact: Joel Emer
- Sun Microsystems Equipment Grants. PI, 2008 & 2009. T2000 SPARC Server (2008) and SPARC Enterprise T5240 Server (2009), total list price: \$53,490

Courses Taught

Average weighted instructor rating: **3.4 out of 4**. Average # of students taught per semester: 44 students.

- Spring 2009 – CIS 371: Digital Systems Organization and Design, 40 students (inst. rating: 3.18/4)
- Fall 2008 – CIS 501: Computer Architecture, 46 students (inst. rating: 3.25/4)
- Spring 2008 – CIS 371: Digital Systems Organization and Design, 47 students (inst. rating: 3.14/4)
- Fall 2007 – sabbatical
- Spring 2007 – CSE 372: Digital Systems Organization and Design Lab, 43 students (3.59/4)
- Fall 2006 – CSE 240: Introduction to Computer Architecture, 89 students (inst. rating: 3.68/4)
- Spring 2006 – CSE 372: Digital Systems Organization and Design Lab, 32 students (inst. rating: 3.56/4)
- Fall 2005 – CIS 501: Computer Architecture, 30 students (inst. rating: 3.07/4)
- Spring 2005 – CIS 700/008 Special Topic: Hardware Support for Security, 14 students (inst. rating: 3.33/4)
- Fall 2004 – CSE 240: Introduction to Computer Architecture, 93 students (inst. rating: 3.17/4) – co-taught with E Lewis

- Spring 2004 – CIS 700/002 Special Topic: Multiprocessor Computer Architecture & Server Workloads, 9 students (inst. rating: 3.56/4)
- University of Wisconsin: Fall 1996 & Spring 1997 – CS 302: Algebraic Language Programming

Course Development

- Redesigned (with E. Lewis) “CSE240: Introduction to Computer Architecture” with the goal of creating a relevant, broad, and exciting course to retain and attract potential majors (this course is required by all CIS-affiliated degrees, including DMD, BAS, BSE, and CE). Our initial experiences with this new course have been extremely positive. Course ratings are high, and many students listed this course as their favorite course on a survey of our CS majors.
- Overhauled “CSE372: Digital Systems Organization and Design Lab” to create a hands-on lab via replacing simulation-based projects with a design project using actual programmable hardware prototyping boards. Worked with undergraduate TAs to develop the course projects, tutorials, and Verilog code for hardware I/O devices such as a video monitor output and keyboard input.

Students, Advising, and Dissertation Committees

PhD Graduates

- Sebastian Burckhardt (co-advised with Rajeev Alur), 2007 – first employment: Microsoft Research

Current Graduate Student Advised

- Colin Blundell, matriculated 2003, completed WPE-I, WPE-II, proposed, PhD expected 2010.
Recipient of IBM Graduate Fellowship for 2009-2010
- Arun Raghavan, matriculated 2006, completed WPE-I, WPE-II
- Sela Mador-Haim (co-advised with Rajeev Alur), matriculated 2007, completed WPE-I, WPE-II
- Santosh Nagarakatte, matriculated 2007, completed WPE-I

Dissertation Committees

- Tingting Sha (advisor: Amir Roth), expected 2009
- Peng Li (advisor: Steve Zdancewic), 2008
- Anne Weinberger Bracy (advisor: Amir Roth), 2008
- Vlad Petric (advisor: Amir Roth), 2007
- Marc Corliss (advisor: E Lewis), 2006

Undergraduate Senior Thesis Projects Supervised

- 2006-2007: Peter Hornyack (2nd place departmental award winner)
- 2005-2006: Joe Devietti, Travis Nidosik

Undergraduate Summer Researchers

- Summer 2009: Andres Velazquez, Evan Benshetler, and Michajlo Matijkiw
- Summer 2006: Peter Hornyack (initially employed by Cisco Systems, now a PhD student at University of Washington)
- Summer 2005: Joe Devietti (now a PhD student at University of Washington)

University Activities and Service

- Penn Departmental Service
 - Computer Engineering Program Committee, AY 2009/2010
 - Computing Committee, AY 2004/2005, 2005/2006, 2006/2007, 2007/2008
 - Systems Faculty Hiring Sub-Committee, AY 2004/2005 (Co-chair), 2005/2006
 - Space Committee, AY 2004/2005, 2005/2006, 2006/2007
 - Graduate Admissions Committee, Spring 2004, Spring 2009
- Penn School of Engineering and Applied Science (SEAS) Service
 - SEAS Computing Committee, AY 2005/2006, AY 2006/2007
- University Service
 - Hearings Panel for the Faculty Grievance Commission, 2009
 - Penn Reading Project Discussion Leader, 2006

Professional Activities and Service

- Program Committees
 - MULTIPROG 2010 – 3rd Workshop on Programmability Issues for Multicore Computers
 - ASPLOS 2010 – 15th International Conference on Architectural Support for Programming Languages and Operating Systems
 - MICRO 2009 – 42nd IEEE/ACM International Symposium on Microarchitecture
 - ICS 2009 – 23rd International Conference on Supercomputing
 - TRANSACT 2009 – 4th ACM SIGPLAN Workshop on Transactional Computing
 - Top Picks 2009 – IEEE Micro's Top Picks 2009
 - ISCA 2008 – 35th International Symposium on Computer Architecture
 - TRANSACT 2008 – 3rd ACM SIGPLAN Workshop on Transactional Computing
 - MULTIPROG 2008 – 1st Workshop on Programmability Issues for Multicore Computers
 - PPOPP 2008 – Symposium on Principles and Practice of Parallel Programming
 - MICRO 2007 – 40th IEEE/ACM International Symposium on Microarchitecture
 - ISCA 2007 – 34th International Symposium on Computer Architecture
 - ISPASS 2007 – International Symposium on Performance Analysis of Systems and Software
 - IPDPS 2007 – The 2007 IEEE International Parallel and Distributed Processing Symposium
 - HiPC 2006 – 13th IEEE International Conference on High Performance Computing
 - ICPP 2006 – The 2006 International Conference on Parallel Processing
 - WMPI 2006 – 4th Workshop on Memory Performance Issues
- External Review Committees
 - ISCA 2010 – 37th International Symposium on Computer Architecture
 - ISCA 2009 – 36th International Symposium on Computer Architecture
- Reviewer for the International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), International Symposium on Computer Architecture (ISCA), International Symposium on High Performance Computer Architecture (HPCA), International Symposium on Microarchitecture (MICRO), International Conference on Supercomputing (ICS), IEEE Computer, IEEE Micro, IEEE Transactions on Computers (ToC), and IEEE Transactions on Parallel and Distributed Systems (TPDS), ACM Transactions on Architecture and Code Optimization (TACO).
- Member: ACM (since 1993), IEEE Computer Society (since 1997)
- Previous maintainer of the *WWW Computer Architecture Home Page*, which receives over 100,000 hits a year. (<http://www.cs.wisc.edu/arch/www/>)

Open-Source Software Distributions

- SoftBound, 2009 – <http://www.cis.upenn.edu/acg/softbound/> – SoftBound is a compile-time transformation for enforcing spatial safety of unmodified C code. Softbound was coded primarily by Santosh Nagarakatte as part of a collaborative project with Jianzhou Zhao, Steve Zdancewic, and Milo M. K. Martin.
- FeS₂, 2008 – <http://fes2.cs.uiuc.edu/> – FeS₂ is a full-system execution-driven timing-first micr-simulator for x86. It builds upon Simics, PTLSim, and GEMS’s Ruby multiprocessor memory system simulator. FeS₂ itself was developed in a collaboration between Naveen Neelakantam and Craig Zilles from the University of Illinois at Urbana-Champaign and Colin Blundell, Joe Devietti, and Milo M. K. Martin from the University of Pennsylvania.
 - As of Aug. 2009, over three hundred messages have been posted to FeS₂’s e-mail list.
- CheckFence, 2007 – <http://checkfence.sourceforge.net/> – CheckFence is a SAT-based formal verification tool that analyzes C code implementing concurrent data types on multiprocessors (concurrent queues, sets etc.) with respect to a selected memory model. Checkfence was created as part of Sebastian Burckhardt’s PhD dissertation, which was co-advised by Rajeev Alur and Milo M. K. Martin.
- Multifacet’s General Execution-driven Multiprocessor Simulator (GEMS) infrastructure, 2005 – <http://www.cs.wisc.edu/gems/>
 - As of April 2009, over 50 academic papers have used GEMS, 2000 users have registered and downloaded GEMS, and 5000 messages have been posted to the GEMS mailing list.
 - Sun Microsystems created a version of GEMS modified to simulate the best-effort transactional memory of Sun’s Rock processor (as mentioned in an article in *EE Times* “Sun rallies industry around Rock CPU” on 01/30/2008).

Patents

- *US 6,981,097: Token based cache-coherence protocol.* Milo M. K. Martin, Mark D. Hill, and David A. Wood. Filed March 2003 / Issued December 2005.
- *US 6,883,070: Bandwidth-adaptive, hybrid, cache-coherence protocol.* Milo M. K. Martin, Daniel J. Sorin, Mark D. Hill, and David A. Wood. Filed November 2001 / Issued April 2005. (Listed in the Microprocessor Report “Patent Watch” column, June 2005)

Court Testimony

- Expert witness testimony regarding the definition of “computer” as defined by the federal Computer Fraud and Abuse Act (CFAA). *GWR Medical v. Baez*, Civil No. 07-1103, U.S. Federal Court, Eastern District of Pennsylvania, February 12, 2008.

Presentations

Secure Low-Level Programming via Hardware-Assisted Memory-Safe C

- Microsoft Research – Redmond, WA – December 2009 (Scheduled)
- VMWare – Palo Alto, CA – November 2009 (Scheduled)
- Stanford University – Palo Alto, CA – November 2009 (Scheduled)
- Princeton University – Princeton, NY – October 2009
- University of Texas – Austin, TX – October 2009
- University of Michigan – Ann Arbor, MI – October 2009

HardBound: Architectural Support for Spatial Safety of the C Programming Language

- IBM T.J. Watson Research Center – December 2008
- NJ Programming Languages and Systems Seminar (NJPLS) – March 2008

Panel member for Workshop on Exploiting Concurrency Efficiently and Correctly (EC²) co-located with Computer Aided Verification (CAV) – July 2008

Transactional Memory's Subtle Semantics and Unrestricted Implementation

- Microsoft Research – Redmond, WA – January 2007
- Massachusetts Institute of Technology (MIT) – Cambridge, MA – December 2006
- Intel – Hudson, MA – November 2006
- Princeton University – Princeton, NJ – November 2006
- Intel – Santa Clara, CA – September 2006

Designing Verifiable Multicores: Formal Verification and its Impact on the Snooping versus Directory Protocol Debate

- Intel's Novel Verification and Validation Solution Research Symposium – September 2006
- Invited presentation at the International Conference on Computer Design (ICCD) – October 2005

Panel member of WDDD 2005's panel on deconstructing transactional memory – June 2005

Token Coherence: Decoupling Performance and Correctness

- University of California at Berkeley – Berkeley, CA – April 2003
- Georgia Tech – Atlanta, GA – April 2003
- University of California at San Diego – La Jolla, CA – April 2003
- Duke University – Durham, NC – April 2003
- Carnegie Mellon University – Pittsburgh, PA – April 2003
- University of Illinois – Urbana, IL – March 2003
- University of Pennsylvania – Philadelphia, PA – February 2003
- Northwestern University – Evanston, IL – February 2003
- University of Minnesota – Minneapolis, MN – February 2003
- Intel – Portland, OR – February 2003
- Intel – Santa Clara, CA – February 2003
- Sun Microsystems – Sunnyvale, CA – February 2003

Bandwidth Adaptive Snooping

- Intel & HP/Compaq Joint Seminar – Shrewsbury, MA – September 2002
- HP/Compaq – Marlboro, MA – September 2002
- University of Texas – Austin, TX – December 2001
- IBM Austin Research Lab (ARL) – Austin, TX – December 2001
- University of Minnesota – Minneapolis, MN – September 2001

Publications

Copies of these papers can be found at <http://www.cis.upenn.edu/~milom/>. Citation count data from Google Scholar. **In total, my papers have received over 1400 citations.**

Author key: *Penn*, Student

Journal Publications

1. *Token Tenure and PATCH: A Predictive/Adaptive Token Counting Hybrid*. Arun Raghavan, Colin Blundell, and **Milo M. K. Martin**. ACM Transactions on Architecture and Code Optimization (ACM TACO), “Accepted pending minor revisions”.
2. *NoSQ: Store-Load Communication without a Store Queue*. Tingting Sha, **Milo M. K. Martin**, and Amir Roth, **IEEE Micro’s “Top Picks of 2006” Issue**, Volume 27, Number 1, pages 106–113, January-February 2007. 18 citations. One of 11 papers selected as a top pick from the top architecture conference of 2006.
3. *Subtleties of Transactional Memory Atomicity Semantics*. Colin Blundell, E Christopher Lewis, and **Milo M. K. Martin**, Computer Architecture Letters (CAL), Volume 5, Number 2, November 2006. 53 citations.
4. *Token Coherence: A New Framework for Shared-Memory Multiprocessors*. **Milo M. K. Martin**, Mark D. Hill, and David A. Wood, **IEEE Micro’s “Top Picks of 2003” Issue**, Volume 23, Number 6, pages 108–116, November-December 2003. 17 citations. One of 15 papers selected as a top pick from the top architecture conference of 2003.
5. *Simulating a \$2M Commercial Server on a \$2K PC*. Alaa R. Alameldeen, **Milo M. K. Martin**, Carl J. Mauer, Kevin E. Moore, Min Xu, Daniel J. Sorin, Mark D. Hill and David A. Wood, **IEEE Computer**, Volume 36, Number 2, pages 50–57, February 2003. 102 citations.
6. *Specifying and Verifying a Broadcast and a Multicast Snooping Cache Coherence Protocol*. Daniel J. Sorin, Manoj Plakal, Anne E. Condon, Mark D. Hill, **Milo M. K. Martin** and David A. Wood, IEEE Transactions on Parallel and Distributed Systems (**IEEE TPDS**), Volume 13, Number 6, pages 556–578, June 2002. 35 citations.

Refereed Archival Conference Publications

1. *InvisiFence: Performance-Transparent Memory Ordering in Conventional Multiprocessors*. Colin Blundell, **Milo M. K. Martin**, and Tom Wenisch. Proceedings of the 36th International Symposium on Computer Architecture (**ISCA**), pages 233–244, June 2009. 43 of 210 submissions accepted (20%).
2. *SoftBound: Highly Compatible and Complete Spatial Memory Safety for C*. Santosh Nagarakatte, Jianzhou Zhao, **Milo M. K. Martin**, and Steve Zdancewic. Proceedings of ACM SIGPLAN Conference on Programming Language Design and Implementation (**PLDI**), pages 245–258 June 2009. 41 of 196 submissions accepted (21%).
3. *Token Tenure: PATCHing Token Counting Using Directory-Based Cache Coherence*. Arun Raghavan, Colin Blundell, and **Milo M. K. Martin**. Proceedings of the 41st International Symposium on Microarchitecture (**MICRO**), pages 47–58, November 2008. 40 of 210 submissions accepted (19%). 3 citations.

4. *HardBound: Architectural Support for Spatial Safety of the C Programming Language*. Joe Devietti, Colin Blundell, **Milo M. K. Martin**, and Steve Zdancewic. Proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), pages 103–114, March 2008. 31 of 127 submissions accepted (24%). 4 citations.
5. *Making the Fast Case Common and the Uncommon Case Simple in Unbounded Transactional Memory*. Colin Blundell, Joe Devietti, E Christopher Lewis, and **Milo M. K. Martin**. Proceedings of the 34th International Symposium on Computer Architecture (**ISCA**), pages 24–34, June 2007. 46 of 204 submissions accepted (23%). 51 citations.
6. *CheckFence: Checking Consistency of Concurrent Data Types on Relaxed Memory Models*. Sebastian Burckhardt, Rajeev Alur, and **Milo M. K. Martin**. Proceedings of the ACM SIGPLAN Conference on Programming Language Design and Implementation (**PLDI**), pages 12–21, June 2007. 45 of 178 submissions accepted (25%). 22 citations.
7. *NoSQ: Store-Load Communication without a Store Queue*. Tingting Sha, **Milo M. K. Martin**, and Amir Roth. Proceedings of the 39th International Symposium on Microarchitecture (**MICRO**), pages 285–296, December 2006. 42 of 174 submissions accepted (24%). 18 citations.
8. *Bounded Model Checking of Concurrent Data Types on Relaxed Memory Models: A Case Study*. Sebastian Burckhardt, Rajeev Alur, and **Milo M. K. Martin**. Proceedings of Computer-aided Verification (**CAV**), pages 489–502, August 2006. 35 of 121 regular submissions accepted (29%). 5 citations.
9. *Scalable Store-Load Forwarding via Store Queue Index Prediction*. Tingting Sha, **Milo M. K. Martin**, and Amir Roth. Proceedings of the 38th International Symposium on Microarchitecture (**MICRO**), pages 159–170, November 2005. 29 of 147 submissions accepted (20%). 33 citations.
10. *Formal Verification and its Impact on the Snooping versus Directory Protocol Debate*. **Milo M. K. Martin**. Proceedings of the International Conference on Computer Design (**ICCD**), pages 543–449, October 2005. **Invited Paper**. 101 of 313 non-invited submissions accepted (32%). 8 citations.
11. *Improving Multiple-CMP Systems Using Token Coherence*. Michael R. Marty, Jesse D. Bingham, Mark D. Hill, Alan J. Hu, **Milo M. K. Martin**, and David A. Wood. Proceedings of the International Symposium on High Performance Computer Architecture (**HPCA**), pages 328–339, February 2005. 28 of 181 submissions accepted (15%). 53 citations.
12. *Verifying Safety of a Token Coherence Implementation by Parametric Compositional Refinement*. Sebastian Burckhardt, Rajeev Alur, and **Milo M. K. Martin**. Sixth International Conference on Verification, Model Checking and Abstract Interpretation (**VMCAI**), pages 130–145, January 2005. 27 of 92 submissions accepted (29%). 5 citations.
13. *Using Speculation to Simplify Multiprocessor Design*. Daniel J. Sorin, **Milo M. K. Martin**, Mark D. Hill, and David A. Wood. Proceedings of the 18th International Parallel and Distributed Processing Symposium (**IPDPS**), pages 75–84, April 2004. 142 of 447 submissions accepted (32%). 2 citations.
14. *Token Coherence: Decoupling Performance and Correctness*. **Milo M. K. Martin**, Mark D. Hill, and David A. Wood. Proceedings of the 30th International Symposium on Computer Architecture (**ISCA**), pages 182–193, June 2003. 37 of 184 submissions accepted (20%). 110 citations.

15. *Using Destination-Set Prediction to Improve the Latency/Bandwidth Tradeoff in Shared Memory Multiprocessors*. **Milo M. K. Martin**, Pacia J. Harper, Daniel J. Sorin, Mark D. Hill, and David A. Wood. Proceedings of the 30th International Symposium on Computer Architecture (**ISCA**), pages 206–217, June 2003. 37 of 184 submissions accepted (20%). 59 citations.
16. *SafetyNet: Improving the Availability of Shared Memory Multiprocessors with Global Checkpoint/Recovery*. Daniel J. Sorin, **Milo M. K. Martin**, Mark D. Hill, and David A. Wood. Proceedings of the 29th International Symposium on Computer Architecture (**ISCA**), pages 123–134, May 2002. 27 of 180 submissions accepted (15%). 130 citations.
17. *Bandwidth Adaptive Snooping*. **Milo M. K. Martin**, Daniel J. Sorin, Mark D. Hill, and David A. Wood. Proceedings of the 8th International Symposium on High Performance Computer Architecture (**HPCA**), pages 251–262, February 2002. 26 of 130 submissions accepted (20%). 44 citations.
18. *Correctly Implementing Value Prediction in Microprocessors that Support Multithreading or Multiprocessing*. **Milo M. K. Martin**, Daniel J. Sorin, Harold W. Cain, Mark D. Hill, and Mikko H. Lipasti, Proceedings of the 34th International Symposium on Microarchitecture (**MICRO**), pages 328–337, December, 2001. 29 of 144 submissions accepted (20%). 31 citations.
19. *Timestamp Snooping: An Approach for Extending SMPs*. **Milo M. K. Martin**, Daniel J. Sorin, Anastassia Ailamaki, Alaa R. Alameldeen, Ross M. Dickson, Carl J. Mauer, Kevin E. Moore, Manoj Plakal, Mark D. Hill, and David A. Wood. Proceedings of the 9th International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), pages 25–36, November 2000. 24 of 114 submissions accepted (21%). 35 citations.
20. *Exploiting Dead Value Information*. **Milo M. Martin**, Amir Roth, and Charles Fischer. Proceedings of the 30th Annual International Symposium on Microarchitecture (**MICRO**), pages 125–135, December 1997. 35 of 103 submissions accepted (34%). 85 citations.

Newsletters, Posters, and Refereed Workshop Publications

1. *Securing Hardware Platforms Against Malicious Through Static Analysis* Matthew Hicks, Samuel T. King, **Milo M. K. Martin**, and Jonathan M. Smith. ACM Symposium on Operating Systems Principles Work In Progress Session, Oct 2009
2. *Specifying Relaxed Memory Models for State Exploration Tools*. Sela Mador-Haim, Rajeev Alur, and **Milo M. K. Martin**. Position paper for the workshop on (EC)2: Exploiting Concurrency Efficiently and Correctly, June 2009
3. *FeS₂: A Full-system Execution-driven Simulator for x86*. Naveen Neelakantam, Colin Blundell, Joe Devietti, **Milo M. K. Martin** and Craig Zilles. Poster session of the International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS Poster**), 2008.
4. *Multifacet’s General Execution-driven Multiprocessor Simulator (GEMS) Toolset*. **Milo M. K. Martin**, Daniel J. Sorin, Bradford M. Beckmann, Michael R. Marty, Min Xu, Alaa R. Alameldeen, Kevin E. Moore, Mark D. Hill, and David A. Wood. SIGARCH Computer Architecture News (**CAN**), Volume 22, Number 4, pages 92–99, September 2005. 301 citations.
5. *Deconstructing Transactional Semantics: The Subtleties of Atomicity*. Colin Blundell, E Christopher Lewis, and **Milo M. K. Martin**. Workshop on Duplicating, Deconstructing, and Debunking (**WDDD**), June 2005. 85 citations.

6. *Evaluating Non-deterministic Multi-threaded Commercial Workloads*. Alaa R. Alameldeen, Carl J. Mauer, Min Xu, Pacia J. Harper, **Milo M. K. Martin**, Daniel J. Sorin, Mark D. Hill and David A. Wood. Workshop On Computer Architecture Evaluation using Commercial Workloads (CAECW), February 2002. 51 citations.
7. *Characterizing a Java Implementation of TPC-W*. Todd Bezenek, Trey Cain, Ross Dickson, Timothy Heil, **Milo Martin**, Collin McCurdy, Ravi Rajwar, Eric Weglarz, Craig Zilles and Mikko Lipasti. Third Workshop on Computer Architecture Evaluation Using Commercial Workloads (CAECW), January 2000. 22 citations.

Technical Reports (not published elsewhere)

1. *Terabit Edge Research Activity (TERA)*. J. M. Smith and **Milo M. K. Martin**, Technical Report AFRL-RY-WP-TR-2008-1254, Air Force Research Laboratory, October 2008.
2. *Unrestricted Transactional Memory: Supporting I/O and System Calls within Transactions*. Colin Blundell, E Christopher Lewis, and **Milo M. K. Martin**, Technical Report CIS-06-09, Department of Computer and Information Science, University of Pennsylvania, Philadelphia, PA, April 2006. 33 citations.
3. *Fast Checkpoint/Recovery to Support Kilo-Instruction Speculation and Hardware Fault Tolerance*. Daniel J. Sorin, **Milo M. K. Martin**, Mark D. Hill, and David A. Wood, Technical Report CS-TR-2000-1420, Dept. of Computer Sciences, University of Wisconsin, Madison, WI, October 2000. 18 citations.

Media

- Quoted in the *MIT Technology Review* article “Intel’s New Strategy: Power Efficiency”, June 2006 (http://www.techreview.com/printer_friendly_article.aspx?id=16943)

Miscellaneous Information

- Erdos number: 3 (Paul Erdos to Michael Saks to Anne Condon to me)