

Computer and Information Science Department
University of Pennsylvania
3330 Walnut Street, 603 Levine Hall
Philadelphia, PA 19104-6389

215.573.0175
amir@cis.upenn.edu
<http://www.cis.upenn.edu/~amir/>

Education

- 2001 **Doctorate of Philosophy in Computer Science**
University of Wisconsin-Madison, Madison, WI
Thesis title: Pre-Execution via Speculative Data-Driven Multithreading.
- 1997 **Master of Science in Computer Science**
University of Wisconsin-Madison, Madison, WI
- 1994 **Bachelor of Science in physics and Bachelor of Arts in Computer Science**
Yale University, New Haven, CT
magna cum laude

Positions Held

- 2009– Undergraduate Program Chair
Computer and Information Science Department, University of Pennsylvania
- 2007– **Associate Professor**
Computer and Information Science Department, University of Pennsylvania
- 2001–2007 **Assistant Professor**
Computer and Information Science Department, University of Pennsylvania

Research Interests

My research focuses improving the performance and performance-efficiency of conventional sequential programs. My current projects include latency-tolerant checkpoint-based processor designs, scalable in-flight data memory systems, and non-blocking multi-threading substrates.

Teaching Experience

- CIS 240: Introduction to Computer Systems (Fall 2008, 2009)
- CIS 372: Computer Organization and Design Lab (Spring 2009, 2008, 2006, 2005, 2004)
- CIS 371: Computer Organization and Design (Spring 2007, 2006, 2005, 2004)
- CIS 501: Introduction to Computer Architecture (Fall 2007, 2006, 2004, 2003, 2002, 2001)

Theses Supervised

- May 2009 Tingting Sha, Doctorate of Philosophy
Thesis: “Exploiting Memory Dependence Prediction to Simplify the Store-Load Datapath”
First employment: nVIDIA Corporation
- Dec. 2008 Anne Bracy, Doctorate of Philosophy
Thesis: “Mini-Graph Processing”
First employment: Intel Corporation
- Apr. 2007 Vlad Petric, Doctorate of Philosophy
Thesis: “RENO: Rename-Based Instruction Optimization”
First employment: Google, Inc.

Representative Refereed Publications

CPROB: Checkpoint Processing with Opportunistic Minimal Recovery

Andrew Hilton, Neeraj Eswaran, and Amir Roth

Proc. 18th International Conference on Parallel Architectures and Compilation Techniques (**PACT'09**), Sep. 14–16, 2009.

Decoupled Store Completion and Silent Deterministic Replay: Enabling Scalable Memory Systems for CPR/CFP Processors.

Andrew Hilton and Amir Roth

Proc. 36th International Symposium on Computer Architecture (**ISCA'09**), Jun. 20–24, 2009.

iCFP: Tolerating All-Level Cache Misses in In-Order Processors

Andrew Hilton and Amir Roth.

Proc. 15th International Symposium on High Performance Computer Architecture (**HPCA'09**), Feb. 16–18, 2009.

Serialization Aware Mini-Graph Selection.

Anne Bracy and Amir Roth.

Proc. 39th International Symposium on Microarchitecture (**MICRO'06**), pages 171–182, Dec. 11–13, 2006.

Scalable Store-Load Forwarding via Store Queue Index Prediction.

Tingting Sha, Milo M. K. Martin, and Amir Roth.

Proc. 38th International Symposium on Microarchitecture (**MICRO'05**), pages 159–170, Nov. 12–16, 2005.

RENO: A Rename Based Instruction Optimizer.

Vlad Petric, Tingting Sha, and Amir Roth.

Proc. 32nd International Symposium on Computer Architecture (**ISCA'05**), pages 98–102, Jun 4–8, 2005.

Store Vulnerability Window (SVW): Re-Execution Filtering for Enhanced Load Optimization.

Amir Roth.

Proc. 32nd International Symposium on Computer Architecture (**ISCA'05**), pages 458–468, Jun 4–8, 2005.

Dataflow Minigraphs: Amplifying Superscalar Capacity and Bandwidth.

Anne Bracy, Prashant Prahald, and Amir Roth.

Proc. 37th International Symposium on Microarchitecture (**MICRO'04**), pages 18–29, Dec. 4–8, 2004.

DISE: A Programmable Macro-Engine for Customizing Applications.

Marc L. Corliss, E Christopher Lewis, and Amir Roth.

Proc. 30th International Symposium on Computer Architecture (**ISCA'03**), pages 362–373, Jun. 9–11, 2003.

A Quantitative Framework for Pre-Execution Thread Selection.

Amir Roth and Gurindar S. Sohi.

Proc. 35th International Symposium on Microarchitecture (**MICRO'02**), pages 430–441, Nov. 18–22, 2002.

Grant Awards

- | | |
|-----------|--|
| 2008 | Intel Corporation Research Council Grant (\$40,000)
“Unifying, Simplifying, and Amplifying Checkpoint-Based Processors” |
| 2006–2009 | NSF CPA award CCF-0541292 (\$400,000)
“ON-Core: Single-Thread Performance via Multi-Core Aggregation” |
| 2004–2006 | Intel Corporation Research Council Grant (\$120,000)
“Exploiting Dataflow Mini-Graphs in Superscalar Processors” |
| 2003–2006 | NSF CSA award CCF-0311199 (\$240,000)
“DISE: A New Hardware-Software Interface for Customizing Application Execution” |
| 2003–2008 | NSF CAREER award CCF-0238203 (\$400,000)
“Correctness-Performance Partitioned (CPP) Architectures” |