

Curriculum Vitae¹

Rajeev Alur

Address

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Personal Information

Date of birth: March 5, 1966.
Citizen of the United States.
Married with two children.

Research Interests

Theories and tools for high-level modeling, design, and analysis of embedded software systems
Hybrid (discrete + continuous) systems, Formal methods, Model checking, Software verification
Logic in computer science, Distributed computing

Education

Ph.D. in Computer Science (August 1991)
Stanford University, Stanford.
Thesis: *Techniques for automatic verification of real-time systems*

Bachelor of Technology in Computer Science (May 1987)
Indian Institute of Technology, Kanpur, India.

Employment

- July 2003 onwards: Zisman Family Professor of Computer and Information Science, University of Pennsylvania.
- July 2001 onwards: Professor, Department of Computer and Information Science, University of Pennsylvania.
- July 1999–June 2001: Associate Professor with tenure, Department of Computer and Information Science, University of Pennsylvania.
- July 1997–June 1999: Associate Professor without tenure, Department of Computer and Information Science, University of Pennsylvania.
- September 1991–June 1997: Member of Technical Staff, Computing Sciences Research Center, Bell Laboratories, Murray Hill.

¹Updated October 2009

Visiting Positions

- July 2006 onwards, Consulting Scientist, NEC Labs America, Princeton, NJ.
- July 1997–August 2001: Part-time Member of Technical Staff, Computing Sciences Research Center, Bell Laboratories, Murray Hill.
- August 1996 - June 1997: Visiting Faculty, Department of Electrical Engineering and Computer Science, University of California, Berkeley.
- January - May 1995: Visiting Faculty, Department of Computer Science, Columbia University, New York.
- June - September 1990: Summer Intern, IBM Almaden Research Center, San Jose.
- March - May 1989: Visiting Researcher, Department of Applied Mathematics, The Weizmann Institute of Science, Rehovot, Israel.
- May - July 1986, and May - August 1987: Software Development Engineer, Kale Consultants, Pune, India.

Honors

- The inaugural CAV (Computer Aided Verification) Award for *fundamental contributions to the theory of real-time systems verification*, 2008.
- Best Paper Award, *8th ACM Conference on Embedded Software (EMSOFT)*, 2008.
- Fellow of the ACM, 2007.
- Fellow of the IEEE, 2008.
- ACM Distinguished Lecturer, 2006-08.
- Endowed Professorship: Zisman Family Professor of Computer and Information Science, University of Pennsylvania, 2003.
- Highly cited researcher, Institute for Scientific Information (Thomson-ISI), January 2005.
- National Science Foundation Information Technology Research Award, 2001.
- Alfred P. Sloan Faculty Fellowship, 1999–2001.
- National Science Foundation Faculty Early Career Development Award, 1998.
- President of India Gold Medal for Academic Excellence, Indian Institute of Technology, Kanpur, 1987.

Teaching

- Automata, Computability, and Complexity (CIS 262, undergraduate). University of Pennsylvania, Fall 2008 and Fall 2009.
- Theory of Computation (CIS 511, graduate). University of Pennsylvania, Spring 2005, Spring 2006, Spring 2007, and Spring 2008.
- Principles of Embedded Computation (CIS 540, graduate). University of Pennsylvania, Fall 2009.
- Logic in Computer Science (CSE 482, undergraduate). University of Pennsylvania, Fall 2004 and Fall 2005.

- Operating Systems (CSE 380, undergraduate). University of Pennsylvania, Fall 2001 and Fall 2002.
- Operating Systems Lab (CSE 381, undergraduate). University of Pennsylvania, Fall 2001.
- Data Structures and Algorithms (CSE 220, undergraduate). University of Pennsylvania, Spring 1998, Spring 1999, and Spring 2000.
- Multi-processor Programming (CIS 640, graduate). University of Pennsylvania, Spring 2009.
- Computer-Aided Verification (CIS 673, graduate). University of Pennsylvania, Fall 1997, Fall 1999, Spring 2003, and Fall 2006, and Columbia University, Spring 1995.
- Program Analysis (CIS 670, graduate). University of Pennsylvania, Fall 2007.
- Hybrid Systems (CIS 640/EE 601, graduate). University of Pennsylvania, Fall 2000.
- Embedded Software (CIS 640, graduate). University of Pennsylvania, Fall 1998 and Spring 2002.

Research Group

Postdoctoral researchers

1. Thao Dang (January 2001–December 2001, now at CNRS, France)
2. Radu Grosu (October 1998–August 2000, now on CS faculty at Stony Brook University)
3. Aditya Kanade (June 2007 - June 2009, now on CS faculty at Indian Institute of Science, Bangalore, India)
4. Supratik Mukhopadhyay (June 2001–July 2002, now on CS faculty at Utah State University)
5. George Pappas (August 1999–February 2000, now on ESE faculty at University of Pennsylvania)
6. Madhusudan Parthasarathy (January 2002–November 2004, now on CS faculty at University of Illinois at Urbana-Champaign)
7. Gera Weiss (July 2006 – June 2009, now on CS faculty at Ben Gurion University, Israel)

PhD students

1. Mikhail Bernadsky (PhD Spring 2008, now at Microsoft Search Labs)
2. Sebastian Burckhardt (PhD Summer 2007, co-supervised with Milo Martin, now at Microsoft Research)
3. Pavol Cerny (PhD Summer 2009, now a postdoctoral researcher at Institute of Science and Technology, Austria)
4. Swarat Chaudhury (PhD Summer 2007, Winner of the Rubinoff Award for the best PhD Thesis, Winner of the 2007 ACM SIGPLAN Dissertation Award, now on CS faculty at Pennsylvania State University)
5. Franjo Ivancic (PhD Fall 2003, Winner of the Rubinoff Award for the best PhD Thesis, now at NEC Labs America)
6. Salvatore La Torre (PhD Fall 2001, now on CS faculty at University of Salerno, Italy)
7. Sela Mador-Haim (Since Fall 2007)

8. Michael McDougall (PhD Spring 2005, co-supervised with Carl Gunter, now at Grammatech)
9. Wonhong Nam (PhD Spring 2007, now researcher at IST, Pennsylvania State University),
10. Bow-Yaw Wang (PhD Summer 2001, now at Academia Sinica, Taiwan)
11. Zijiang Yang (PhD Fall 2003, now on CS faculty at Western Michigan University)

MS students

Himyanshu Anand (MS 2000)
Arnabnil Bhattacharjee (MS, 1999)
Arun Chandrasekharapuram (MS, 2005)
Gunjan Gupta (MS, 2004)
Minsu Kang (MS 2001)
Jason Simas (MS 2004)

Departmental and University activities

- Director, Embedded Systems Masters Program, 2009–.
- Graduate Group Chair, Department of Computer and Information Science, 2005–2009.
- University Committee on Academic Planning and Budget, 2007–2010.
- Department of Computer and Information Science Colloquium Chair, 2004–2005.
- Computer and Information Science, Graduate Admissions, 1997–2000. Chair, 2000.
- Computer and Information Science, MS Curriculum Revision and initiation of the new Master of Computer and Information Technology Program, 1999–2000.
- School of Engineering and Applied Science, Library Committee, 1997–2000.
- School of Engineering and Applied Science, Faculty Personnel Committee, Member 2001–2002, Chair 2002–2003.
- University Research Council, 1999–2001.
- PhD Thesis Committee: Madhukar Anand, Brian Aydemir, Colin Blundell, Georgios Fainekos, Alwyn Goodloe, Yerang Hur, Hee-Hwan Kwak, Davor Obradovic, Jianping Shi, Insik Shin, Jangwoo Shin, and Mahesh Viswanathan.

Professional Activities

Professional societies

- Chair, ACM SIGBED (Special Interest Group on Embedded Systems), 2005–2007.
- General Chair, IEEE Logic in Computer Science (LICS), 2009–2012.

Editorial board

- ACM Transactions on Embedded Computer Systems, 2003 onwards.
- Formal Methods in System Design, Springer, 1995 onwards.
- Formal Methods Letters, Springer, 2004 onwards.
- International Journal of Foundations of Computer Science, World Scientific, 2002 onwards.
- Logical Methods in Computer Science, 2004 onwards.

Conference Organization

1. Co-organizer, *Exploiting Concurrency Efficiently and Correctly* (EC²), CAV Workshop; Princeton, July 2008, Grenoble, France, July 2009, and Edinburgh, UK, July 2010.
2. Program Chair, *21st IEEE Symposium on Logic in Computer Science* (LICS), Seattle, August 2006.
3. Program Co-chair and Conference Co-chair, *16th International Conference on Computer-Aided Verification* (CAV), Boston, July 2004.
4. Program Co-chair and Conference Co-chair, *Seventh International Workshop on Hybrid Systems: Computation and Control* (HSCC), Philadelphia, March 2004.
5. Program Co-chair and Conference Co-chair, *Third International Workshop on Embedded Software* (EMSOFT), Philadelphia, October 2003.
6. Program Co-chair and Conference Co-chair, *Eighth International Conference on Computer-Aided Verification* (CAV), New Brunswick, August 1996.
7. Program Co-chair and Conference Co-chair, *DIMACS Workshop on Verification and Control of Hybrid Systems*, New Brunswick, October 1995.

Selected Program committees

1. *International Conference on Computer Aided Verification* (CAV): 2010, 2009, 2008, 2007, 2004, 2003, 2001, 2000, 1998, 1997, 1996, 1995, 1994, 1993, 1992.
2. *ACM SIGPLAN Conference on Programming Language Design and Implementation* (PLDI): 2008.
3. *ACM Conference on Embedded Software* (EMSOFT): 2009, 2007, 2006, 2003, 2002.
4. *ACM Symposium on Principles of Programming Languages* (POPL): 2010.
5. *IEEE Symposium on Foundations of Computer Science* (FOCS): 2006.
6. *International Conference on Hybrid Systems: Computation and Control* (HSCC): 2006, 2004, 2003, 2002, 2001, 2000, 1999, 1998.
7. *International Conference on Tools and Algorithms for the Construction and Analysis of Systems* (TACAS): 2005, 2003, 2001, 1999.
8. *IEEE Real-Time and Embedded Technology and Applications Symposium* (RTAS): 2005.
9. *IEEE Symposium on Logic in Computer Science* (LICS): 2006, 2004, 1999.
10. *IEEE Real-Time Systems Symposium* (RTSS): 2003, 1993.
11. *Annual Conference of the European Association for Computer Science Logic* (CSL): 2002.
12. *International Conference on Concurrency Theory* (CONCUR): 2001.
13. *International Joint Conference on Automated Reasoning* (IJCAR): 2001.
14. *International Colloquium on Automata, Languages, and Programming* (ICALP): 2000.
15. *ACM Symposium on Principles of Distributed Computing* (PODC): 1998.
16. *International Symposium on Automated Technology for Verification and Analysis* (ATVA): 2009, 2007, 2006, 2005.

17. *International Workshop on Formal Modeling and Analysis of Timed Systems (FORMATS)*: 2007, 2006, 2003.
18. *Conference on Foundations of Software Technology and Theoretical Computer Science (FSTTCS)*: 2003.
19. *IFIP International Conference on Theoretical Computer Science (TCS)*: 2008.
20. *International School and Symposium on Formal Techniques in Real-time and Fault-tolerant Systems (FTRTFT)*: 2002, 2000.
21. *International Conference on Verification, Model Checking, and Abstract Interpretation (VMCAI)*: 2003.
22. *ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP)*: 2003.

Other committees

1. ACM Paris Kanellakis Theory in Practice Award Committee, 2007-2010 (Chair, 2008-09).
2. Scientific Council, Digiteo, a research park in France on Communication and Information Technology.
3. Steering committee, *International Workshop on Formal Modeling and Analysis of Timed Systems (FORMATS)*, 2003 onwards.
4. Steering committee, *International Conference on Hybrid Systems: Computation and Control (HSCC)*, 2002 onwards.
5. LICS Test-of-Time Award Committee, 2005–2007 (Chair, 2007).
6. Steering committee, *Workshop on Probabilistic Methods in Verification (PROBMIV)*, 1998–2002.
7. Panelist and/or participant in DARPA/NSF workshops on various initiatives on embedded systems, 1998 onwards.
8. Panelist for National Science Foundation, 1998, 2001, 2002, 2003, 2004, 2006, 2007, 2008, and 2009.
9. Conference committee, *Federated Logic Conference*, New Brunswick, July-August 1996.
10. Working group on formal methods, *ACM Workshop on Strategic Directions in Computing Research*, Boston, June 1996.
11. Working group on concurrency, *ACM Workshop on Strategic Directions in Computing Research*, Boston, June 1996.

External Reviewer on PhD Thesis Committee

Patricia Bouyer (ENS Cachan, France), Jatindra Deka (IIT Kharagpur, India), Victor Du (SUNY Stony Brook), Ansgar Fehnker (University of Nijmegen, Netherlands), Martijn Hendriks (Radboud University, Netherlands), Aditya Kanade (IIT Bombay, India), Martin Lange (LMU Munich, Germany), Flavio Lerda (Carnegie Mellon University), Dejan Nickovic (University of Grenoble, France), Gerardo Schneider (University of Grenoble, France), Bikram Sengupta (SUNY Stony Brook), Vasu Singh (EPFL, Switzerland), Ofer Strichman (Weizmann Inst. of Science, Israel), Stavros Tripakis (University of Grenoble, France).

Journal referee

Acta Informatica, ACM Transactions on Computational Logic, ACM Transactions on Design Automation of Electronic Systems, ACM Transactions on Embedded Computer Systems, ACM Transactions on Programming Languages and Systems, ACM Transactions on Software Engineering and Methodology, Bulletin of Symbolic Logic, Distributed Computing, Formal Aspects of Computing, Formal Methods in System Design, Fundamenta Informaticae, IEEE Parallel & Distributed Technology, IEEE Software, IEEE Transactions on Computers, IEEE Transactions on Computer-Aided Design, IEEE Transactions on Automatic Control, IEEE Transactions on Software Engineering, Information and Computation, Information Processing Letters, International Journal on Foundations of Computer Science, Journal of the ACM, Journal of Algorithms, Journal of Automated Reasoning, Journal of Computer and System Sciences, Journal of Discrete Event Dynamic Systems, Journal of Logic and Computation, Journal of Parallel and Distributed Computing, Mathematics of Control Systems and Signals, Mathematical Structures in Computer Science, Science of Computer Programming, and Theoretical Computer Science.

Proposal reviewer

Air-Force Office for Scientific Research, Engineering and Physical Sciences Research Council, United Kingdom, Israel Science Foundation, National Science Foundation, Natural Sciences and Engineering Research Council, Canada, Science Foundation of Ireland, The Netherlands Computer Science Research Foundation, The Netherlands Organization for Scientific Research, and Swiss National Science Foundation.

Professional societies

ACM, SIGACT, SIGBED, SIGSOFT, IEEE Computer Society.

Invited Lectures

1. Architecture-aware analysis of concurrent software. Intel Symposium on Hardware and Software Co-design and Co-verification, Haifa, Israel, September 2009.
2. Temporal reasoning about program executions. The European Joint Conferences on Theory and Practice of Software (ETAPS), York, UK, March 2009.
3. Marrying words and trees. *Logic and Algorithms*, Edinburgh, UK, July 2008.
4. Software model checking. The Milner Lecture, Laboratory for Foundations of Computer Science, University of Edinburgh, July 2008.
5. Architecture-aware analysis of concurrent software. Distinguished Lecture Series, Max-Planck Institute for Software Systems, Saarbrücken, Germany, July 2008.
6. Marrying words and trees. *12th International Conference on Algebraic Methodology and Software Technology (AMAST)*, Urbana, July 2008.
7. Architecture-aware analysis of concurrent software. Jon Postel Distinguished Lecturer, Department of Computer Science, University of California at Los Angeles, November 2007.
8. Architecture-aware analysis of concurrent software. Distinguished Lecture Series, Department of Computer Science, University of Illinois at Urbana-Champaign, October 2007.
9. Marrying words and trees. *Computer Science Symposium in Russia (CSR'07)*, Ekaterinburg, Russia, September 2007.

10. Concurrent executions on relaxed memory models: Challenges and opportunities for software model checking. *14th International Workshop on Model Checking Software (SPIN)*, Berlin, Germany, July 2007.
11. Principles of embedded computation. Distinguished colloquium, Department of Computer Science and Engineering, Arizona State University, April 2007.
12. Software model checking. Distinguished colloquium, Department of Computer Science and Engineering, Pennsylvania State University, November 2006.
13. Logics, automata, and algorithms for analysis of structured programs. Minicourse, *Marktoberdorf Summer School on Software and System Reliability and Security*, Germany, August 2006.
14. Model checking: From tools to theory. *25MC: 25 Years of Model Checking*, Seattle, August 2006.
15. Hybrid systems modeling for regulatory pathways. *FLoC Workshop on Logic in Systems Biology (LSB)*, Seattle, August 2006.
16. Games for formal design and verification of reactive systems. Keynote lecture, *Fourth ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE)*, Napa, July 2006.
17. Nested words and trees. Tutorial, Workshop on Games and Verification, Newton Institute for Mathematical Sciences, Cambridge, UK, July 2006.
18. Adding nesting structure to words. Keynote lecture, *10th International Conference: Developments in Language Theory (DLT)*, Santa Barbara, June 2006.
19. The benefits of exposing calls and returns. Keynote lecture, Joint session of *16th International Conference on Concurrency Theory (CONCUR)* and *12th International SPIN Workshop on Model Checking of Software (SPIN)*, San Francisco, August 2005.
20. Modeling and analysis of hybrid and embedded systems. Minicourse at the Lipari School, Formal Methods: Theory and Practice, *17th International School for Computer Science Researchers*, Lipari Island, Italy, June 2005.
21. Games for formal design and verification of reactive systems. Keynote lecture, *Second International Symposium on Automated Technology for Verification and Analysis (ATVA)*, Taipei, Taiwan, November 2004.
22. Formal modeling and analysis of hybrid systems. Tutorial, *Second International Symposium on Automated Technology for Verification and Analysis (ATVA)*, Taipei, Taiwan, November 2004.
23. Timed automata and model checking. *Fourth International Summer School on Formal Methods for the Design of Computer, Communication, and Software Systems: Real Time*, Bertinoro, Italy, September 2004.
24. Analysis of scenario-based requirements. Distinguished Colloquium Series, Department of Electrical Engineering and Computer Science, Vanderbilt University, Nashville, November 2003.
25. Software synthesis from hybrid automata. *Monterrey Workshop on Software Engineering for Embedded Systems*, Chicago, September 2003.
26. Formal modeling and analysis of hybrid systems. *2003 Illinois International Multiconference on Measurement, Modelling, and Evaluation of Computer-Communication Systems*, Urbana, September 2003.

27. Analysis of hierarchical state machines. *Verification: Theory in Practice, Workshop in honor of Zohar Manna*, Taormina, Italy, July 2003.
28. Analysis of Message Sequence Charts. *CRM Workshop on Formal Methods*, Montreal, Canada, September 2002.
29. Reachability Analysis of Hybrid Systems using Predicate Abstraction. *18th Workshop on Mathematical Foundations of Programming Semantics (MFPS)*, New Orleans, March 2002.
30. Hybrid Systems: Modeling and Verification. *IFIP Working Group 2.3 School on Formal Software Engineering*, Pune, India, January 2002.
31. Hierarchical Hybrid Modeling of Embedded Systems. *First International Workshop on Embedded Software (EMSOFT)*, Tahoe City, October 2001.
32. Hybrid systems: Modeling and Verification. One-day minicourse for *Fifth Dynamics Workshop*, Brussels, July 2001.
33. Exploiting modularity in model checking. *11th International Conference on Concurrency Theory (CONCUR)*, State College, August 2000.
34. CHARON: Modular specification and simulation of hybrid systems. Keynote speaker at *Dagstuhl Seminar on Probabilistic Methods in Verification*, Wadern, Germany, May 2000.
35. Model checking of real-time and hybrid systems. *11th International Conference on Computer-Aided Verification (CAV)*, Trento, Italy, July 1999.
36. Efficient formal verification of hierarchical descriptions. *18th Annual Conference on Foundations of Software Technology and Theoretical Computer Science (FSTTCS)*, Chennai, India, December 1998.
37. Model Checking. EECS Departmental Colloquium, Lehigh University, October 1998.
38. Model checking of probabilistic real-time systems. *Workshop on Probabilistic Methods in Verification (PROBMIV)*, Indianapolis, June 1998.
39. Modeling and analysis of hybrid systems. Joint session of *12th International Workshop on Qualitative Reasoning (QR)* and *Ninth International Workshop on Principles of Diagnosis (DX)*, Cape Cod, May 1998.
40. Formal verification of timed circuits. *Fifth ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU)*, Austin, December 1997.
41. Controller synthesis for timed and hybrid systems. *Fifth International Hybrid Systems Workshop*, Notre Dame, September 1997.
42. Timed automata. *NATO ASI Summer School on Verification of Digital and Hybrid Systems*, Antalya, Turkey, May 1997.
43. Modularity for timed and hybrid systems. *School on Methods and Tools for the Verification of Infinite State Systems*, Grenoble, France, March 1997.
44. Model checking for real-time and hybrid systems. *Workshop on Applied Formal Methods*, Hyderabad, India, December 1996.
45. Partial-order logics. *DIMACS Workshop on Partial-Order Methods in Verification*, Princeton, July 1996.
46. Reactive modules. *ONR Workshop on Automated Formal Methods*, Oxford, UK, June 1996.
47. Algorithmic verification of timed and hybrid systems. *Eighth Conference on Formal Description Techniques (FORTE)*, Montreal, Canada, October 1995.

48. Timing analysis in COSPAN. *DIMACS Workshop on Verification and Control of Hybrid Systems*, New Brunswick, October 1995.
49. Hybrid automata. *11th International Conference on Analysis and Optimization of Systems*, Sophia-Antipolis, France, June 1994.
50. Real-time systems: Verification. *AMAST Workshop on Real-Time Systems (ARTS)*, Iowa City, November 1993.
51. Model checking for real-time systems. *Fourth International Conference on Computer-Aided Verification (CAV)*, Elounda, Greece, July 1993.
52. Automatic verification of real-time systems. *Third Conference on Concurrency Theory (CONCUR)*, Stony Brook, August 1992.
53. Modeling and verifying real-time systems. *Workshop on temporal and real-time specification*, Berkeley, August 1990.

Seminar Talks

Bellcore (March 1991 and September 1992), Carnegie Mellon University (October 1992, December 2001), Columbia University (October 1994), Cornell University (February 1991, September 1992, and October 1993), EPFL, Switzerland (July 2005), IBM T.J. Watson Research Center (October 1994 and July 2007), Indian Institute of Technology at Kanpur (January 2008), Indian Institute of Technology at Mumbai (January 2003), Intel Design Labs (August 1998), Loyola University of Chicago (April 1994), McMaster University (May 2002), Microsoft Research (May 2009), MIT (January 1994, April 1997, October 1999, August 2005, and March 2006), NEC Research Labs (July 1999 and September 2006), Pennsylvania State University (March 1991), Rice University (April 1995), Rutgers University (April 2004), SRI International (April 1991, August 1996), State University of New York at Stony Brook (November 1995), Stanford University (May 1990, February 1991, March 1992, and April 1993), University of California at Berkeley (September 1990, September 1996, November 1996, and August 1998), University of California at Santa Barbara (January 1991), University of Delaware (March 2009), University of Paris (July 2003), University of Pennsylvania (March 1995, March 1997, November 1997, October 1999, October 2000, October 2002, October 2003, November 2003, September 2005, September 2006, September 2008, and October 2009), and Verimag, Grenoble, France (July 2005).

Software

1. **CheckFence** (with Sebastian Burckhardt and Milo Martin): a SAT-based verification tool for analyzing implementations of concurrent data types with respect to user specified memory model (<http://checkfence.sourceforge.net/>).
2. **Jist** (with students): a tool for automatic extraction of behavioral interfaces from Java classes (see www.cis.upenn.edu/jist/).
3. **CHARON** (with I. Lee, O. Sokolsky, and others): a modeling and analysis environment for hierarchical hybrid systems (see www.cis.upenn.edu/mobies/charon/).
4. **HERMES** (with students): a model checker for communicating hierarchical state machines (see www.cis.upenn.edu/sdrl/hermes/).
5. **MOCHA** (with T. Henzinger and others): a model checking environment for reactive systems (available at www.cis.upenn.edu/~mocha/).

6. **Timed COSPAN** (with R. Kurshan): Model checker to debug a description of a real-time system against correctness requirements.
7. **MSC Analyzer** (with G. Holzmann, B. Kernighan, and D. Peled): A CASE tool for creating, editing, and analyzing message sequence charts for specifying requirements for the telecommunication software.

Patents

Timing verification by successive approximation: An algorithm for timing analysis, that is implemented in COSPAN, and gives heuristic improvements in the time and space requirements of the verification task. US Patent 5483470, 1996 (with A. Itai, R. Kurshan, and M. Yannakakis).

Model checking of hierarchical state machines: Algorithms for analysis of hierarchical state machines. US Patent 6324,496, 2001 (with M. Yannakakis).

Model checking of message flow diagrams: Methodology and algorithms for automated analysis of scenario-based requirements. US Patent 6516306, 2003 (with M. Yannakakis).

Implied message sequence charts: Methodology and algorithms for inferring implied scenarios from input requirements. US Patent 6681264, 2004 (with K. Etessami and M. Yannakakis).

Programmable payment cards: system and method for using open APIs to provide integrated security policies and flexible management and customization of payment instruments (with C.A. Gunter, M. McDougall, and A. Goodloe); pending.

Books

Computer-Aided Verification 1999 (with T. Henzinger) See draft at www.cis.upenn.edu/cis673/

Edited Volumes

1. Logical Methods in Computer Science, Special Issue of Selected Papers of LICS 2006, 2009 (with R. Jagadeesan and L. Libkin).
2. Formal Methods in System Design, Vol. 32, No. 1, 2008 (with G.J. Pappas).
3. Proceedings, 21st Annual IEEE Symposium on Logic in Computer Science, 2006.
4. ACM Transactions on Embedded Computer Systems, Special issue on Embedded Software, Vol. 4, No. 4, 2005 (with I. Lee).
5. Computer Aided Verification, Proceedings of the 16th International Conference. Lecture Notes in Computer Science 3114, Springer 2004 (with D. Peled).
6. Hybrid Systems: Computation and Control, Seventh International Workshop, HSCC 2004, Proceedings. Lecture Notes in Computer Science 2993, Springer, 2004 (with G. Pappas).
7. Embedded Software, Third International Conference, EMSOFT 2003, Proceedings. Lecture Notes in Computer Science 2855, Springer, 2003 (with I. Lee).
8. Information and Computation, Vol. 164, No. 2, 2001 (with T. Henzinger).
9. Formal Methods in System Design, Vol 15, No. 1, July 1999 (with T. Henzinger).
10. Formal Methods in System Design, Vol 14, No. 3, May 1999 (with T. Henzinger).
11. CAV 96: Computer-Aided Verification. Lecture Notes in Computer Science 1102, Springer Verlag, 1996 (with T. Henzinger).

12. Hybrid Systems III: Verification and Control. Lecture Notes in Computer Science 1066, Springer Verlag, 1996 (with T. Henzinger and E. Sontag).

Refereed Journal Publications

1. Adding nesting structure to words, *Journal of the ACM (JACM)* **56(3)**, 2009 (with P. Madhusudan).
2. First-order and temporal logics for nested words, *Logical Methods in Computer Science (LMCS)* **4(4: 11)**, 2008 (with M. Arenas, P. Barcelo, K. Etessami, N. Immerman, and L. Libkin). Invited submission to LICS 2007 special issue.
3. Automatic symbolic compositional verification by learning assumptions, *Formal Methods in System Design* **32(3)**, pp. 207–234, 2008 (with W. Nam and P. Madhusudan). Invited submission to special issue on Learning and Verification.
4. Dispatch sequences for embedded control models, *Journal of Computer and System Sciences* **73(2)**, pp. 156–170, 2007 (with A. Chandrashekarapuram). Invited submission to special issue on real-time and embedded systems.
5. Predicate abstraction for reachability analysis of hybrid systems, *ACM Transactions on Embedded Computer Systems* **5(1)**, pp. 152–199, 2006 (with T. Dang and F. Ivancic).
6. Compositional modeling and refinement for hierarchical hybrid systems, *Journal of Logic and Algebraic Programming* **68(1-2)**, pp. 105–128, 2006 (with R. Grosu, I. Lee, and O. Sokolsky).
7. Deciding global partial order properties. *Formal Methods in System Design* **26**, pp. 7–25, 2005 (with K. McMillan and D. Peled).
8. Analysis of recursive state machines, *ACM Transactions on Programming Languages and Systems* **27(4)**, pp. 786–818, 2005 (with M. Benedikt, K. Etessami, P. Godefroid, T. Reps, and M. Yannakakis).
9. Modular strategies for recursive game graphs, *Theoretical Computer Science* **354**, pp. 230–249, 2006 (with S. La Torre and P. Madhusudan). Invited submission for TACAS’03 special issue.
10. Counter-example guided predicate abstraction of hybrid systems, *Theoretical Computer Science* **354**, pp. 250–271, 2006 (with T. Dang and F. Ivancic). Invited submission for TACAS’03 special issue.
11. Symbolic computational techniques for solving games, *Springer International Journal on Software Tools for Technology Transfer* **7(2)**, pp. 118–128, 2005 (with P. Madhusudan and W. Nam). Invited submission for BMC’03 special issue.
12. Optimal paths in weighted timed automata, *Theoretical Computer Science* **318(3)**, pp. 297–322, 2004 (with S. La Torre and G. Pappas).
13. Polyhedral flows in hybrid automata. *Formal Methods in System Design* **24(3)**, pp. 261–280, 2004 (with S. Kannan and S. La Torre).
14. Modular refinement of hierarchic state machines, *ACM Transactions on Programming Languages and Systems* **26(2)**, pp. 339–369, 2004 (with R. Grosu).
15. Formal specification and analysis of the computer-assisted resuscitation algorithm (CARA) infusion pump control system, *Software Tools for Technology Transfer* **5(4)**, pp. 308–319, 2004 (with D. Arney, E. Gunter, I. Lee, J. Lee, W. Nam, F. Pearce, S. van Albert, and J. Zhou). Invited submission to special issue on formal methods for medical devices.

16. Inference of message sequence charts, *IEEE Transactions on Software Engineering* **29(7)**, pp. 623–633, 2003 (with K. Etessami and M. Yannakakis).
17. Hierarchical modeling and analysis of embedded systems, *Proceedings of the IEEE* **91(1)**, pp. 11–28, 2003 (with T. Dang, J. Esposito, Y. Hur, F. Ivancic, V. Kumar, I. Lee, P. Mishra, G. Pappas, and O. Sokolsky). Invited submission to special issue on embedded systems.
18. A framework and architecture for multirobot coordination, *International Journal of Robotic Research*, to appear (with R. Fierro, A. Das, J. Spletzer, Y. Hur, J. Esposito, G. Grudic, V. Kumar, I. Lee, J. Ostrowski, G. Pappas, J. Southall, C.J. Taylor). Invited submission to ISER’00 special issue.
19. Deterministic generators and games for LTL fragments, *ACM Transactions on Computational Logic* **5(1)**, pp. 1–25, 2004 (with S. La Torre).
20. Realizability and verification of MSC graphs, *Theoretical Computer Science* **331**, pp. 97–114, 2005 (with K. Etessami and M. Yannakakis). Invited submission for ICALP’01 special issue.
21. Modeling and analyzing biomolecular networks, *IEEE Computing in Science and Engineering* **4(1)**, pp. 20–31, 2002 (with C. Belta, V. Kumar, M. Mintz, G. Pappas, H. Rubin, and J. Schug). Invited submission to special issue on Biocomputation.
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24. Parametric temporal logic for model measuring, *ACM Transactions on Computational Logic*, **2(3)**, pp. 388–407, 2001 (with K. Etessami, S. La Torre, and D. Peled).
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27. Model-checking of correctness conditions for concurrent objects. *Information and Computation*, **160(1-2)**, pp. 167–188, 2000 (with K. McMillan and D. Peled). Invited submission to LICS’96 special issue.
28. Undecidability of partial order logics. *Information Processing Letters* **69(3)**, pp. 137–143, 1999 (with D. Peled).
29. Finitary fairness. *ACM Transactions on Programming Languages and Systems* **20(6)**, pp. 1171–1194, 1998 (with T. Henzinger).
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35. The benefits of relaxing punctuality. *Journal of the ACM* **43(1)**, pp. 116-146, 1996 (with T. Feder and T. Henzinger).
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37. Automatic symbolic verification of embedded systems. *IEEE Transactions on Software Engineering* **22(3)**, pp. 181–201, 1996 (with T. Henzinger and P. Ho).
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3. Trends and challenges in algorithmic software verification. *Verified Software: Theories, Tools, Experiments*, pp. 245–250, LNCS 4171, Springer, 2005.
4. Adding nesting structure to words, *Developments in Language Theory: 10th International Conference*, LNCS 4036, pp. 1–13, 2006 (with P. Madhusudan).
5. Decision problems for timed automata: A survey, *Formal Methods for the Design of Real-Time Systems*, LNCS 3185, pp. 1–24, 2004 (with P. Madhusudan).
6. Formal analysis of hierarchical state machines, *Verification: Theory and Practice, Essays dedicated to Zohar Manna*, LNCS 2772, pp. 42–66, 2004.

7. Hierarchical hybrid modeling of embedded systems, *First International Workshop on Embedded Software* (EMSOFT), LNCS 2211, pp. 14–31, 2001 (with T. Dang, J. Esposito, R. Fierro, Y. Hur, F. Ivancic, V. Kumar, I. Lee, P. Mishra, G. Pappas, and O. Sokolsky).
8. Timed automata. *Proceedings of the 11th International Conference on Computer-Aided Verification* (CAV), LNCS 1633, pp. 8–22, 1999.
9. Symbolic analysis of hybrid systems. *Proceedings of the 37th IEEE Conference on Decision and Control* (CDC), 1997 (with T. Henzinger and H. Wong-Toi).
10. Timed Automata. *Verification of Digital and Hybrid Systems*, NATO ASI Series Vol. 170, (M.K. Inan, R.P. Kurshan, eds.), pp. 233–264, 2000.
11. Alternating-time temporal logic. *Compositionality—the significant difference* (W.-P. de Roever, H. LangMaack, A. Pnueli, eds.), LNCS 1536, pp. 23–60, 1998 (with T. Henzinger and O. Kupferman).
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17. Time for logic. *SIGACT News* **22(3)**, pp. 6–12, 1991 (with T. Henzinger).
18. Logics and models of real time: A survey. *Real-Time: Theory in Practice* (J. de Bakker, C. Huizing, W.-P. de Roever, G. Rozenberg, eds.), LNCS 600, pp. 74–106, 1991 (with T. Henzinger).
19. Verifying automata specifications of probabilistic real-time systems. *Real-Time: Theory in Practice* (J. de Bakker, C. Huizing, W. de Roever, G. Rozenberg, eds.), LNCS 600, pp. 28–44, 1991 (with C. Courcoubetis and D. Dill).

Refereed Conference Publications

1. Temporal reasoning for procedural programs. *11th International Conference on Verification, Model Checking, and Abstract Interpretation* (VMCAI), 2010.
2. Robust stability of multi-hop networks. *48th IEEE Conference on Decision and Control* (CDC), 2009 (with G. Weiss, A. D’Innocenzo, A.J. Isaksson, K.H. Johansson, and G.J. Pappas).
3. Algorithmic analysis of array-accessing programs, *18th EACSL Annual Conference on Computer Science Logic* (CSL), 2009 (with P. Cerny and S. Weinstein).

4. Scalable scheduling algorithms for wireless networked control systems, *5th Annual IEEE Conference on Automation Science and Engineering (CASE)*, 2009 (with A. D’Innocenzo, G. Weiss, A.J. Isaksson, K.H. Johansson, and G.J. Pappas).
5. Generating and analyzing symbolic traces of Simulink/Stateflow models, *21st International Conference on Computer-Aided Verification (CAV)*, LNCS 5643, pp. 430–445, 2009 (with A. Kanade, F. Ivancic, S. Ramesh, S. Sankaranarayanan, and K.C. Shashidhar).
6. Automated analysis of Java methods for confidentiality, *21st International Conference on Computer-Aided Verification (CAV)*, LNCS 5643, pp. 173–187, 2009 (with P. Cerny).
7. Modeling and analysis of multi-hop control networks, *15th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS)*, 2009 (with A. D’Innocenzo, K.H. Johansson, G.J. Pappas, and G. Weiss).
8. On Omega-languages defined by mean-payoff conditions, *12th International Conference on Foundations of Software Science and Computation Structures (FoSSaCS)*, LNCS 5504, pp. 333–347, 2009 (with A. Degorre, O. Maler, and G. Weiss).
9. Specification and analysis of network resource requirements of control systems, *12th International Conference on Hybrid Systems: Computation and Control (HSCC)*, LNCS 5469, pp. 381–395, 2009 (with G. Weiss, S. Fischmeister, and M. Anand).
10. Symbolic analysis for improving simulation coverage of Simulink/Stateflow models, *8th Annual ACM Conference on Embedded Software (EMSOFT)*, pp. 89–98, 2008 (with A. Kanade, S. Ramesh, and K.C. Shashidhar).
11. RTComposer: A framework for real-time components with scheduling interfaces, *8th Annual ACM Conference on Embedded Software (EMSOFT)*, pp. 159–168, 2008 (with G. Weiss).
12. Ranking automata and games for prioritized requirements, *20th International Conference on Computer-Aided Verification (CAV)*, LNCS 5123, pp. 240–253, 2008 (with A. Kanade and G. Weiss).
13. Regular specifications of resource requirements for embedded control software, *14th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS)*, pp. 159–168, 2008 (with G. Weiss).
14. Instrumenting C programs with nested word monitors, *14th International Workshop on Model Checking Software (SPIN)*, LNCS 4595, pp. 279–283, 2007 (with S. Chaudhuri).
15. First-order and temporal logics for nested words, *22nd IEEE Symposium on Logic in Computer Science (LICS)*, pp. 151–160, 2007 (with M. Arenas, P. Barcelo, K. Etessami, N. Immerman, and L. Libkin).
16. Marrying words and trees, *26th ACM Symposium on Principles of Database Systems (PODS)*, pp. 233–242, 2007.
17. Checkfence: Checking consistency of concurrent data types on relaxed memory models, *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, pp. 12–21, 2007 (with S. Burckhardt and M.M.K. Martin).
18. Model checking of tree logics with path equivalences, *13th International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS)*, LNCS 4424, pp. 664–678, 2007 (with P. Cerny and S. Chaudhuri).
19. Automata based interfaces for control and scheduling, *10th International Conference on Hybrid Systems: Computation and Control (HSCC)*, LNCS 4416, pp. 601–613, 2007 (with G. Weiss).

20. Symbolic analysis of GSMP models with one stateful clock, *10th International Conference on Hybrid Systems: Computation and Control (HSCC)*, LNCS 4416, pp. 90–103, 2007 (with M. Bernadsky).
21. Branching pushdown tree automata, *26th Annual Conference on Foundations of Software Technology and Theoretical Computer Science (FSTTCS)*, LNCS 4337, pp. 393–404, 2006 (with S. Chaudhuri).
22. Time-triggered implementations of dynamic controllers, *6th Annual ACM Conference on Embedded Software (EMSOFT)*, pp. 2–11, 2006 (with T. Nghiem, G. Pappas, and A. Girard).
23. Learning-based symbolic assume-guarantee reasoning with automatic decomposition, *Fourth International Symposium on Automated Technology for Verification and Analysis (ATVA)*, LNCS 4218, pp. 170–185, 2006 (with W. Nam).
24. Languages of nested trees, *18th International Conference on Computer-Aided Verification (CAV)*, LNCS 4144, pp. 329–342, 2006 (with S. Chaudhuri and P. Madhusudan).
25. Bounded model checking of concurrent data types on relaxed memory models: A case study, *18th International Conference on Computer-Aided Verification (CAV)*, LNCS 4144, pp. 489–502, 2006 (with S. Burckhardt and M.M.K. Martin).
26. Preserving secrecy under refinement, *33rd International Colloquium on Automata, Languages, and Programming (ICALP)*, LNCS 4052, pp. 107–118, 2006 (with P. Cerny and S. Zdancevic).
27. Bounded model checking of GSMP models of stochastic real-time systems, *Ninth International Conference on Hybrid Systems: Computation and Control (HSCC)*, LNCS 3927, pp. 19–33, 2006 (with M. Bernadsky).
28. A fixpoint calculus for local and global program flows, *33rd ACM Symposium on Principles of Programming Languages (POPL)*, pp. 153–165, 2006 (with S. Chaudhuri and P. Madhusudan).
29. Quantifying the gap between embedded control models and time triggered implementations, *26th IEEE Real-Time Systems Symposium (RTSS)*, pp. 111–120, 2005 (with A. Girard, G. Pappas and H. Yazarel).
30. Congruences for visibly pushdown languages, *32nd International Colloquium on Automata, Languages, and Programming (ICALP)*, LNCS 3580, pp. 1102–1114, 2005 (with V. Kumar, P. Madhusudan, and M. Viswanathan).
31. Symbolic compositional verification by learning assumptions, *17th International Conference on Computer-Aided Verification (CAV)*, LNCS 3576, pp. 548–562, 2005 (with P. Madhusudan and W. Nam).
32. On-the-fly reachability and cycle detection for recursive state machines, *11th International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS)*, LNCS 3440, pp. 61–76, 2005 (with S. Chaudhuri, K. Etessami, and P. Madhusudan).
33. Dispatch sequences for embedded control models, *11th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS)*, pp. 508–518, 2005 (with A. Chandrashekharam).
34. Perturbed timed automata, *Eighth International Conference on Hybrid Systems: Computation and Control (HSCC)*, LNCS 3414, pp. 70–85, 2005 (with S. La Torre and P. Madhusudan).
35. Verifying safety of a token coherence implementation by parametric compositional refinement, *Sixth International Conference on Verification, Model Checking, and Abstract Interpretation (VMCAI)*, LNCS 3385, pp. 130–145, 2005 (with S. Burckhardt and M. Martin).

36. Synthesis of interface specifications from Java classes, *32nd ACM Symposium on Principles of Programming Languages (POPL)*, pp. 98–109, 2005 (with P. Cerny, P. Madhusudan, and W. Nam).
37. A model-based approach to integrating security policies for embedded devices, *Fourth ACM Conference on Embedded Software (EMSOFT)*, pp. 211–219, 2004 (with M. McDougall and C. Gunter).
38. Variable reuse for efficient image computation, *Fifth International Conference on Formal Methods in Computer-Aided Design (FMCAD)*, LNCS 3312, pp. 430–444, 2004 (with Z. Yang).
39. Structured modeling of concurrent stochastic hybrid systems, *Joint Conference on Formal Modeling and Analysis of Timed Systems and Formal Techniques in Real-Time and Fault Tolerant Systems (FORMATS-FTRTFT)*, LNCS 3253, pp. 309–324, 2004 (with M. Bernadsky and R. Sharykin).
40. Optimal reachability in weighted timed games, *31st International Colloquium on Automata, Languages, and Programming (ICALP)*, LNCS 3142, pp. 122–133, 2004 (with M. Bernadsky and P. Madhusudan).
41. Visibly pushdown languages, *36th ACM Symposium on Theory of Computing (STOC)*, pp. 202–211, 2004 (with P. Madhusudan).
42. A temporal logic of nested calls and returns, *Tenth International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS)*, LNCS 2988, pp. 467–481, 2004 (with K. Etessami and P. Madhusudan).
43. Compression of partially ordered strings, *14th International Conference on Concurrency Theory (CONCUR)*, LNCS 2761, pp. 42–56, 2003 (with S. Chaudhuri, K. Etessami, S. Guha, and M. Yannakakis).
44. Playing games with boxes and diamonds, *14th International Conference on Concurrency Theory (CONCUR)*, LNCS 2761, pp. 128–143, 2003 (with S. La Torre and P. Madhusudan).
45. Symbolic computational techniques for solving games, *First International Workshop on Bounded Model Checking (BMC)*, 2003 (with P. Madhusudan and W. Nam).
46. Modular strategies for infinite games on recursive game graphs, *15th International Conference on Computer-Aided Verification (CAV)*, LNCS 2725, pp. 67–79, 2003 (with S. La Torre and P. Madhusudan).
47. Generating embedded software from hierarchical hybrid models, *ACM Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES)*, pp. 171–182, 2003 (with F. Ivancic, J. Kim, I. Lee, and O. Sokolsky).
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50. Progress on reachability analysis of hybrid systems using predicate abstraction *Sixth International Workshop on Hybrid Systems: Computation and Control (HSCC)*, LNCS 2623, pp. 4–19, 2003 (with T. Dang and F. Ivancic).
51. Visual programming for modeling and simulation of biomolecular networks, *Ninth International Conference on High Performance Computing (HiPC)*, LNCS 2552, pp. 702–712, 2002 (with C. Belta, F. Ivancic, V. Kumar, H. Rubin, J. Schug, and J. Web).

52. Predictable programs in barcodes, *ACM International Conference on Compilers, Architectures, and Synthesis of Embedded Systems (CASES)*, 2002 (with A. Goodloe, M. McDougall, and C. Gunter).
53. Exploiting behavioral hierarchy for efficient model checking, *14th International Conference on Computer-Aided Verification (CAV)*, LNCS 2404, pp. 338–342, 2002 (with M. McDougall and Z. Yang).
54. Reachability analysis of hybrid systems via predicate abstraction, *Fifth International Workshop on Hybrid Systems: Computation and Control (HSCC)*, LNCS 2289, pp. 35–48, 2002 (with T. Dang and F. Ivancic).
55. Shared variables interaction diagrams, *16th IEEE International Conference on Automated Software Engineering (ASE)*, pp. 281–288, 2001 (with R. Grosu).
56. Heuristics for hierarchical partitioning with applications to model checking, *11th Advanced Research Working Conference on Correct Hardware Design and Verification Methods (CHARME)*, LNCS 2144, pp. 71–85, 2001 (with O. Moller).
57. Analysis of recursive state machines, *13th International Conference on Computer-Aided Verification (CAV)*, LNCS 2102, pp. 207–220, 2001 (with K. Etessami and M. Yannakakis).
58. Verifying network protocol implementations by symbolic refinement checking, *13th International Conference on Computer-Aided Verification (CAV)*, LNCS 2102, pp. 169–181, 2001 (with B.-Y. Wang).
59. Deterministic generators and games for LTL fragments, *16th IEEE Symposium on Logic in Computer Science (LICS)*, pp. 291 – 302, 2001 (with S. La Torre).
60. Realizability and verification of MSC graphs, *28th International Colloquium on Automata, Languages, and Programming (ICALP)*, LNCS 2076, pp. 797–808, 2001 (with K. Etessami and M. Yannakakis).
61. Mocha: A model checking tool that exploits design structure, *23rd International Conference on Software Engineering (ICSE)*, pp. 835–836, 2001 (with L. de Alfaro, R. Grosu, T.A. Henzinger, M. Kang, R. Majumdar, F. Mang, C.M. Kirsch, and B.-Y. Wang).
62. Compositional refinement of hierarchical hybrid systems, *Fourth International Workshop on Hybrid Systems: Computation and Control (HSCC)*, LNCS 2034, pp. 33–48, 2001 (with R. Grosu, I. Lee, and O. Sokolsky).
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65. A framework and architecture for multirobot coordination *Seventh International Symposium on Experimental Robotics (ISER)*, LNCIS 271, pp. 303–312, 2000 (with A. Das, J. Esposito, R. Fierro, Y. Hur, G. Grudic, V. Kumar, I. Lee, J. Ostrowski, G. Pappas, J. Southall, J. Spletzer, and C. Taylor).
66. Automated refinement checking for asynchronous processes, *Third International Conference on Formal Methods in Computer-Aided Design (FMCAD)*, LNCS 1954, pp. 55-72, 2000 (with R. Grosu and B.-Y. Wang).

67. Efficient reachability analysis of hierarchic reactive machines, *12th International Conference on Computer-Aided Verification (CAV)*, LNCS 1855, pp. 280–295, 2000 (with R. Grosu and M. McDougall).
68. Inference of message sequence charts, *22nd International Conference on Software Engineering (ICSE)*, pp. 304–313, 2000 (with K. Etessami and M. Yannakakis).
69. Modular specifications of hybrid systems in CHARON, *Third International Workshop on Hybrid Systems: Computation and Control (HSCC)*, LNCS 1790, pp. 6–19, 2000 (with R. Grosu, Y. Hur, V. Kumar and I. Lee).
70. Modular refinement of hierarchic state machines, *27th ACM Symposium on Principles of Programming Languages (POPL)*, pp. 390–402, 2000 (with R. Grosu).
71. Formal modeling and analysis of hybrid systems: A case study in multirobot coordination, *FM’99: Proceedings of the World Congress on Formal Methods*, LNCS 1708, pp. 212–232, 1999 (with J. Esposito, M. Kim, V. Kumar, and I. Lee).
72. Model checking of message sequence charts, *Tenth International Conference on Concurrency Theory (CONCUR)*, LNCS 1664, pp. 114–129, 1999 (with M. Yannakakis).
73. “Next” heuristic for on-the-fly model checking, *Tenth International Conference on Concurrency Theory (CONCUR)*, LNCS 1664, pp. 98–113, 1999 (with B.-Y. Wang).
74. Automating modular verification, *Tenth International Conference on Concurrency Theory (CONCUR)*, LNCS 1664, pp. 82–97, 1999 (with L. de Alfaro, T. Henzinger, and F. Mang).
75. Communicating hierarchical state machines, *26th International Colloquium on Automata, Languages, and Programming (ICALP)*, LNCS 1644, pp. 169–178, 1999 (with S. Kannan and M. Yannakakis).
76. Parametric temporal logic for model measuring, *26th International Colloquium on Automata, Languages, and Programming (ICALP)*, LNCS 1644, pp. 159–168, 1999 (with K. Etessami, S. La Torre, and D. Peled).
77. Polyhedral flows in hybrid automata. *Second International Workshop on Hybrid Systems: Computation and Control (HSCC)*, LNCS 1569, pp. 5–18, 1999 (with S. Kannan and S. La Torre).
78. Membership problems for timed and hybrid automata. *19th IEEE Real-Time Systems Symposium (RTSS)*, pp. 254–263, 1998 (with R. Kurshan and M. Viswanathan).
79. Model checking of hierarchical state machines. *Sixth ACM Symposium on Foundations of Software Engineering (FSE)*, pp. 175–188, 1998 (with M. Yannakakis).
80. Alternating refinement relations. *Ninth International Conference on Concurrency Theory (CONCUR)*, LNCS 1466, pp. 163–178, 1998 (with T. Henzinger, O. Kupferman, and M. Vardi).
81. Deciding global partial order properties. *25th International Colloquium on Automata, Languages, and Programming (ICALP)*, LNCS 1443, pp. 41–52, 1998 (with K. McMillan and D. Peled).
82. MOCHA: modularity in model checking. *Tenth International Conference on Computer-Aided Verification (CAV)*, LNCS 1427, pp. 516–520, 1998 (with T. Henzinger, F. Mang, S. Qadeer, S. Rajamani, and S. Tasiran).
83. Symbolic exploration of transition hierarchies. *Fourth International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS)*, LNCS 1384, pp. 330–344, 1998 (with T. Henzinger and S. Rajamani).

84. Alternating-time temporal logic. *38th IEEE Symposium on Foundations of Computer Science (FOCS)*, pp. 100-109, 1997 (with T. Henzinger and O. Kupferman).
85. Modularity for timed and hybrid systems. *Eighth International Conference on Concurrency Theory (CONCUR)*, LNCS 1243, pp. 74–88, 1997 (with T. Henzinger).
86. Partial order reduction in symbolic state space exploration. *Ninth International Conference on Computer-Aided Verification (CAV)*, LNCS 1254, pp. 340–351, 1997 (with R. Brayton, T. Henzinger, S. Qadeer, and S. Rajamani).
87. Model-checking of real-time systems: a telecommunications application. *19th International Conference on Software Engineering (ICSE)*, pp. 514–524, 1997 (with L. Jagadeesan, J. Kott, and J. Von Olnhausen).
88. Verifying abstractions of timed systems. *Seventh International Conference on Concurrency Theory (CONCUR)*, LNCS 1119, pp. 546–562, 1996 (with R. Kurshan and S. Taşiran).
89. Reactive modules. *11th IEEE Symposium on Logic in Computer Science (LICS)*, pp. 207-218, 1996 (with T. Henzinger).
90. Model-checking of correctness conditions for concurrent objects. *11th IEEE Symposium on Logic in Computer Science (LICS)*, pp. 219-228, 1996 (with K. McMillan and D. Peled).
91. An analyzer for message sequence charts. *Second International Workshop on Tools and Algorithms for the Construction and Analysis of Systems (TACAS)*, LNCS 1055, pp. 35–48, 1996 (with G. Holzmann and D. Peled).
92. Local liveness for compositional modeling of fair reactive systems. *Seventh International Conference on Computer-Aided Verification (CAV)*, LNCS 939, pp. 166–179, 1995 (with T. Henzinger).
93. Model-checking of causality properties. *Tenth IEEE Symposium on Logic in Computer Science (LICS)*, pp. 90–100, 1995 (with D. Peled and W. Penczek).
94. Distinguishing tests for nondeterministic and probabilistic machines. *27th ACM Symposium on Theory of Computing (STOC)*, pp. 363–372, 1995 (with C. Courcoubetis and M. Yannakakis).
95. Contention-free complexity of shared memory algorithms. *13th ACM Symposium on Principles of Distributed Computing (PODC)*, pp. 61–70, 1994 (with G. Taubenfeld).
96. The observational power of clocks. *Fifth International Conference on Concurrency Theory (CONCUR)*, LNCS 836, pp. 162–177, 1994 (with C. Courcoubetis and T. Henzinger).
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Research Grants

1. CoPI, NSF award CNS 0931239, “Quantitative analysis and design of control networks,” 9/1/2009–8/31/2012, \$1,500,000 (with I. Lee, R. Mangharam, G.J. Pappas, and A. Ribeiro).
2. PI, NSF award CCF 0915777, “Scalable symbolic analysis of hybrid systems,” 9/1/2009–8/31/2012, \$376,430.
3. PI, NSF award CCF 0905464, “Formal analysis of concurrent software on relaxed memory models,” 9/1/2009–8/31/2012, \$1,200,000 (with M.M.K. Martin).
4. PI, General Motors, “Formal modeling and analysis of hybrid systems,” 6/1/2007–5/31/2009, \$232,741.
5. PI, NSF award CPA 0541149, “Behavioral interfaces for software components,” 9/1/2006–8/31/2009, \$300,000.
6. CoPI, NSF Cybertrust award CNS 0524059, “Resource guided implementation of secure embedded software,” 9/1/2005–8/31/2009, \$1,000,000 (with A. Scedrov and S. Zdancewic).
7. CoPI, NSF award CSR-EHS 0509143, “A hierarchy of models for embedded software,” 8/1/2005–7/31/2008, \$500,000 (with I. Lee and W. Wolf).
8. PI, NSF award CCR-0410662, “Synthesis of embedded software from hybrid models,” 9/1/2004–8/31/2007, \$400,001 (with I. Lee and G. Pappas).
9. PI, NSF award CCR-0401049, “Workshop on hybrid systems,” 4/15/2004–4/15/2005, \$20,000 (with G.J. Pappas).
10. CoPI, NSF award CCR-0318299, “Workshop on embedded software,” 7/15/2003–6/30/2004, \$15,000 (with I. Lee).
11. PI, NSF award CCR-0306382, “Games for formal design and verification of reactive systems,” 6/1/2003–5/31/2006, \$270,000.
12. CoPI, NSF award CCR-0209990, “Third party programmability of embedded systems,” 7/1/2002–6/30/2004, \$180,000 (with C. Gunter).
13. PI, NSF ITR award ITR/SY 0121431, “Formal Design and Analysis of Hybrid Systems,” 9/1/2001–8/31/2006, \$1,000,000 (with G.J. Pappas).
14. CoPI, ARO URI award DAAD19-01-1-0473, “Advanced Tool Integration for Embedded Systems Assurance,” 5/1/2001–4/30/2006, \$4,984,330 (with C. Gunter, S. Kannan, I. Lee, and O. Sokolsky).
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17. PI, SRC (Semiconductor Research Corporation) award 99-TJ-688, “Exploiting hierarchical structure for efficient formal verification,” 7/1/1999–6/30/2002, \$366,000.
18. PI, NSF award CCR99-70925, “Specification, analysis, and testing of scenario-based requirements,” 9/15/1999–8/31/2002, \$215,000.
19. CoPI, DARPA ITO MARS award 130-1303-4-534328, “Control of Multiple Autonomous Robots,” 7/1/1999–6/30/2002, \$1,800,000 (with K. Daniilidis, V. Kumar, I. Lee, C.J. Taylor, and L. Unger).

20. PI, Alfred P. Sloan Faculty Fellowship, 9/1/1999-8/31/2001, \$35,000.
21. PI, NSF CAREER award CCR97-34115, "Computer-aided verification of reactive systems," 7/1/1998-6/31/2002, \$200,000.
22. CoPI, DARPA/NASA grant NAG2-1214, "MOCHA: Modularity in model checking," 5/1/98-4/30/00, \$850,000 (with T.A. Henzinger).