

CIS 540 Fall 2009: Homework 5, Due December 2

Please write your answers succinctly and rigorously. If you have any questions, or if you get stuck on some problem, please contact the TA or the instructor.

1. Consider an asynchronous OR gate with inputs x and y and output z . Assume that initially all variables have 0 value. The event $x?$ denotes toggling of the input wire x , and similarly the event $y?$ denotes the toggling of the input wire y . The gate can change its output by issuing the event $z!$. The timing assumptions are expressed by the following rules 10pts
 - (a) When an input changes at time t_1 , if this change warrants a change in the output (according to the standard logic of OR gate), then the output should be issued at time t_2 such that the delay $t_2 - t_1$ is between 2 to 4 time units (unless the inputs change again during the interval from t_1 to t_2 , if so, see rules below).
 - (b) While a change in the output is pending in the interval $[t_1, t_2]$, if one of the inputs changes again, but this change is consistent with the output change about to happen at time t_2 , then the output should change as scheduled.
 - (c) While a change in the output is pending in the interval $[t_1, t_2]$, if one of the inputs changes at time t in a manner so as to make the change in output inconsistent with the revised inputs, then the behavior depends on the relative difference $t - t_1$: if this is less than 1, then the pending output change is canceled; if it is more than 1, then it's too late, and output change will occur as scheduled at time t_2 , and at that time, another output event is scheduled with a delay of 2 to 4 time units.

Based on this description, design a timed process (as a state machine with one clock variable) that models the OR gate. The process should be input-enabled: it should allow input events to happen at all times.

2. Describe a protocol for solving n -process consensus using using atomic registers (shared variables supporting separate read and write operations) and timing assumptions. State timing assumptions explicitly. Describe the protocol in state machine notation (using mutual exclusion protocol of Figure 6.6 as a guide). Argue (informally) why the protocol meets all the three requirements of consensus. 10pts
3. Consider a non-empty canonical DBM R and an index $1 \leq i \leq k$. Describe clearly how to compute the DBM R' that captures the effect of setting the clock x_i to 0. That is, R' should represent the set of clock valuations v such that $v = u[x_i \mapsto 0]$ for some $u \in R$. 10pts
4. Consider the timed process shown below with 3 clocks. Compute the sets $R_A, R'_A, R_B, R'_B, R_C$ and R'_C of clock values, represented as canonical DBMs such that each of R_A, R_B, R_C captures the possible clock values when the corresponding mode is entered, and each of R'_A, R'_B, R'_C captures the possible clock values as the process waits in the corresponding mode. 10pts

