

CIS 540 Fall 2009: Homework 2, Due October 21

Please write your answers succinctly and rigorously. If you have any questions, or if you get stuck on some problem, please contact the TA or the instructor.

1. (a) Consider the Boolean expression 5pts

$$(x_1 \wedge x_2 \wedge x_3) \vee (\neg x_2 \wedge x_4) \vee (\neg x_3 \wedge x_4)$$

Choose a variable ordering for the variables $\{x_1, x_2, x_3, x_4\}$, and draw the resulting OBDD. Can you reduce the size of the OBDD by reordering the variables?

- (b) Let V be the set $\{x_0, x_1, y_0, y_1, z_0, z_1, c\}$. Choose an appropriate ordering of the variables, and construct the OBDD for the requirement that the output z_1z_0 , together with the carry bit c , is the sum of the inputs x_1x_0 and y_1y_0 . Is your choice of ordering optimal? 5pts
2. We want to design an asynchronous process `Split` that is the dual of `Merge`. The process `Split` has one input channel `in` and two output channels `out1` and `out2`. The messages received on the input channel should be routed to one of the output channels in a nondeterministic manner so that all possible splittings of the input stream are feasible executions.
- (a) Describe precisely all the components of the desired process `Split`. 5pts
- (b) Suppose we want to capture the requirement that the distribution of messages among the two output channels should be, while unspecified, fair in the sense that if infinitely many messages arrive then both output channels should have infinitely many messages output. How would you add fairness specification to your design to capture this requirement? Do we need weak fairness or strong fairness? Why? 5pts
3. Consider the shared object `StickyBit` that supports read and write operations as in case of an atomic register, with some modification. The internal state of a `StickyBit` can be `null`, 0, or 1. The read operation outputs the current value. The write operation has a Boolean (0 or 1) value associated with it: if the current state is `null` then the state is updated to the value of write, but if not (that is, state is already 0 or 1), the value stays unchanged.
- (a) Describe a protocol for solving 2-process consensus using a single `StickyBit`. You may use any number of additional atomic registers if needed. The protocol can be described as a sequence of steps each process executes, and argue informally why the protocol meets all the three requirements of consensus. 5pts
- (b) Can you solve consensus for 3 (or more generally, n) processes using multiple `StickyBit` and `AtomicReg` objects? 5pts
4. Consider the leader election protocol of Section 3.3.1.
- (a) Consider a ring with 16 nodes where the identifiers of the processes in the order in which they are connected are: 25, 3, 6, 15, 19, 8, 7, 14, 4, 22, 21, 18, 24, 1, 10, 23. Which process will be elected as the leader? 5pts
- (b) Describe the best-case and worst-case scenarios for this protocol: describe a scenario in which only one node will stay active after the first round, and describe a scenario in which half of the processes continue to stay active in each phase. 5pts