Name: _____

Intro. to Computer Architecture	**Homework 4**
CSE 240 Autumn 2006	**Due: Wed. 11 October 2006**

Write your answers on these pages. Additional pages may be attached (with staple) if necessary. Please ensure that your answers are legible and *show your work.* Write your name at the top of each page. Due at the ***beginning of class***. Total points: 62

1. [6 Points] **Instruction Encoding.** Suppose a machine encodes instructions in 32 bits according to the following format. Also, suppose the encoding must accommodate 110 opcodes and 28 registers.

   (a) What is the minimum number of bits required to represent the OPCODE field?

   (b) What is the minimum number of bits required to represent each of the register fields (*e.g.*, DR)?

   (c) What is the greatest number of bits that are left for the IMM field? If the IMM field encodes a 2's complement integer, what range of values can be represented with these bits?

2. [12 Points] **LC-3 Instruction Encoding.** For these questions assume the LC-3 instruction encoding (inside the back cover of your textbook). You may also want to consult Appendix A.

   (a) What is the range of values (in decimal) that may be specified by the immediate field in an AND instruction?

   (b) What is the range of values (in decimal) that may be specified by the PCoffset field in a BR instruction?

   (c) What is the range of values (in decimal) that may be specified by the offset field in an LDR instruction?

   (d) What is the relationship between JMP and RET? In particular, why do they have the same bits in the opcode field?

   (e) Give the encoding of two LC-3 instructions that together increment register R3 by 20. Complete the following table.

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Instruction
x3001																	
x3002																	

3. [15 Points] **LC-3 Code.** Suppose you want to write a program consisting of instructions with the behavior described by the operation in the final column of the following table.

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Operation
x3001																	R2 <- M[R1+0]
x3002																	R3 <- M[R1+1]
x3003																	R4 <- NOT R3
x3004																	R4 <- R4 + 1
x3005																	R5 <- R2 + R4
x3006																	BRzp x3009
x3007																	M[R1+2] <- R3
x3008																	BRnzp x3010
x3009																	M[R1+2] <- R2

(a) Give the binary encoding of each instruction in the table. Write your answers in the table, above.

(b) Trace the execution of the above program, starting at x3001, by completing the following table. Give the PC and operation to execute in the first two columns, and give the state of the registers and condition codes *after* the execution of that instruction (**leave an entry blank if it is not changed by the instruction**). The initial state and the effect of the first instruction are given in the first two rows. Assume memory locations x3100 and x3101 contain 14 and 27, respectively.

PC	Operation	R0	R1	R2	R3	R4	R5	R6	R7	CCs	M[x3102]
initial state ⇒		0	x3100	0	3	4	5	6	7		0
x3001	R2 <- M[R1+0]			14						P	

(c) In a sentence, what does this code compute?

4. [16 Points] **LC-3.** The following (bit-level) memory contents represent an LC-3 program.

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Instruction
x3001	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	R1 <- M[R0+0]
x3002	0	1	0	1	0	1	0	0	1	0	1	0	0	0	0	0	
x3003	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	1	
x3004	0	0	0	1	0	1	0	0	1	0	0	0	0	0	0	1	
x3005	0	0	0	1	0	1	1	0	1	1	1	1	1	1	1	1	
x3006	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	
x3007	0	1	1	1	0	1	0	0	0	0	0	0	0	0	1	0	

(a) First, determine what each instruction does. Write this next to each instruction (above) in a manner similar to that of the previous problem.

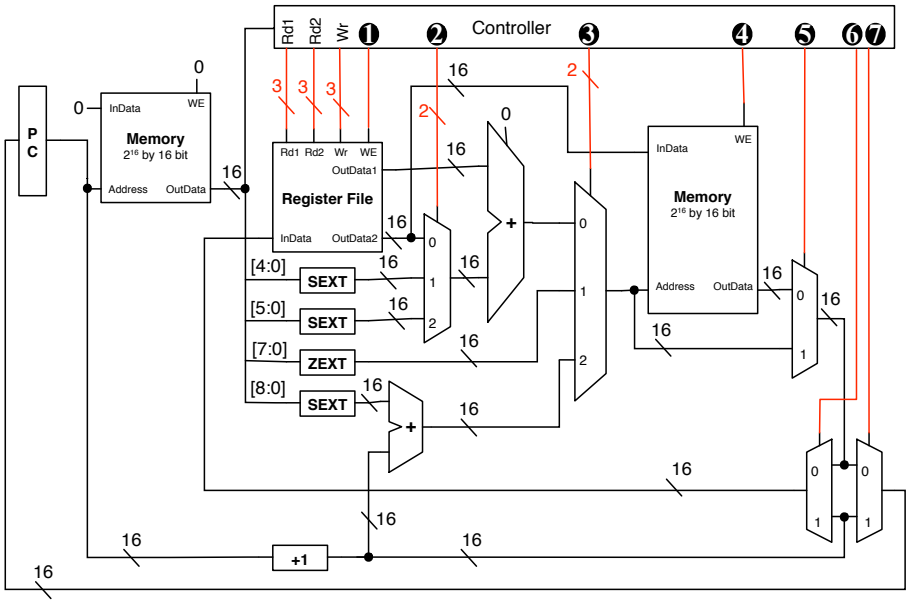
(b) Next, trace the execution of the above program, starting at x3001, by completing the following table. Give the PC and instruction to execute in the first two columns, and give the state of the registers and condition codes *after* the execution of that instruction (**leave an entry blank if it has not been changed by the instruction**). The initial state and the effect of the first instruction are given in the first two rows. Assume memory locations x3100 and x3101 contain 3 and 2, respectively.

PC	Instruction	R0	R1	R2	R3	R4	R5	R6	R7	CCs	M[x3102]
initial state $\Rightarrow$		x3100	1	2	3	4	5	6	7		0
x3001	R1 <- M[R0+0]		3							P	

(c) Describe what this code does, assuming execution starts at address x3001. What registers or memory serve as input to this code? And what registers or memory serve as output? Be very careful in determining the input and output (*i.e.*, just because a register appears in the code does not mean that it is input or output).

(d) Under what circumstances will this program fail to perform its principal task?

5. [12 Points] **LC-3 Data-path.** Consider the single-cycle LC-3 data-path from lecture.



Give the control lines for the instructions in the table, below. In each box, place either a constant (*e.g.*, 2), one or more bits from the instruction (*e.g.*, I[8:6]), or "X" indicating that the value on the control line does not matter.

	Opcode		Registers			Control						
Name	I[15:12]	I[5]	Rd1	Rd2	Wr	❶	❷	❸	❹	❺	❻	❼
ADD	0001	0	I[8:6]	I[2:0]	I[11:9]	1	0	0	0	1	0	1
ADD Immed	0001	1										
LDR	0110	—	I[8:6]	x	I[11:9]	1	2	0	0	0	0	1
LD	0010	—										
STR	0111	—										
ST	0011	—										
LEA	1110	—										
JMP	1100	—	I[8:6]	x	x	0	2*	0	0	1	x	0
JSRR	0100	—										

*Because the low-order 6 bits of the JMP instruction encoding are all zeros, this control signal causes the mux to select 0.

6. [1 Point] **Last and Most Important Question!** Give us your feedback.

   (a) How many hours did you spend on this assignment?

   (b) On a scale of 1-5, how difficult did you find this assignment? (1-easiest, 5-most difficult)

   (c) Do you have any other comments on your experience completing this assignment? What are they?