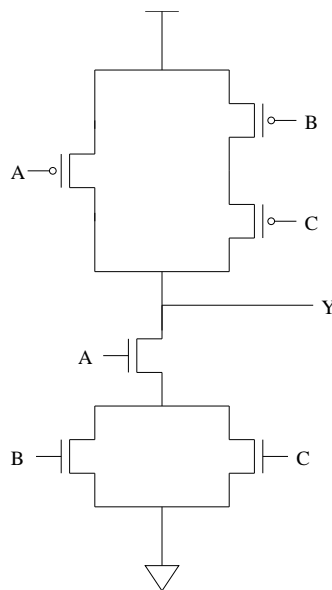


Name: _____

Intro. to Computer Architecture CSE 240 Autumn 2006	Homework 2 Due: Fri. 22 September 2006
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Write your answers on these pages. Additional pages may be attached (with staple) if necessary. Please ensure that your answers are legible and *show your work*. Write your name at the top of each page. Due at the *beginning of class*. Total points: 44.

1. [4 Points] **Complex Gate**. Fill in the truth table for the following complex gate:



A	B	C	Y
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

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2. [8 Points] **Logical Completeness.** NAND is logically complete (*i.e.*, any logic function can be built using only NAND gates). Use the minimum number of NAND gates (and *only* NAND gates) to construct gate-level circuits that compute the following:

(a) NOT

(b) AND

(c) OR

(d) NOR

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3. [18 Points ((4x4) + 2)] **Combinational Logic.** In this question you'll create four different implementations of the same logic function, Z :

A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

- (a) Construct a gate-level logic circuit for Z (above) directly using a PLA.

- (b) How many transistors does your circuit require (assume that n -input NOR and NAND gates have $2n$ transistors; n -input OR and AND gates have $2n + 2$ transistors)? Hint: count only a single inverter for calculating each of \bar{A} , \bar{B} , and \bar{C} .

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(c) Construct a gate-level logic circuit for Z by creating a PLA for the *inverse* of Z (\bar{Z}) and replacing the OR gate with a NOR gate).

(d) How many transistors does your second circuit require (again assuming standard n -input CMOS gates)?

(e) Construct a “minimal” gate-level logic circuit for Z (minimal in terms of transistors) using the standard CMOS gates (and, or, not, nand, nor).

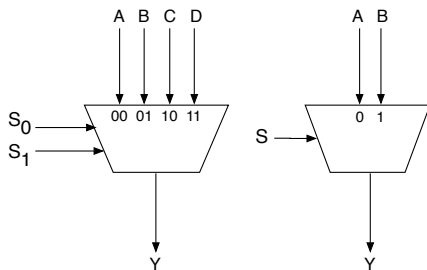
(f) How many transistors does your third circuit require (again, assuming standard n -input CMOS gates)?

(g) Construct a “minimal” CMOS transistor-level circuit for Z (minimal in terms of transistors). Hint: first construct a single complex gate for \bar{Z} .

(h) How many transistors does your transistor-level circuit use?

(i) What can you learn from comparing the number of transistors used by these four different implementations of the same logic function?

4. [5 Points] **Multiplexers.** A one-bit 4-to-1 mux (below, left) selects among four inputs using two selector lines. Specifically, the mux outputs A when the selectors have the value 00 (with S_1 being the high-order bit), B when they have the value 01, C when they have the value 10, and D when they have the value 11. Construct a one-bit 4-to-1 mux (*i.e.*, build a circuit with the behavior of a one-bit 4-to-1 mux) using only one-bit 2-to-1 muxes (below, right). Be sure to label the inputs ($A, B, C, D, S_0,$ and S_1) and output (Y).



5. [8 Points (3+4+1)] **Logic Design.** Your task is to design the logic to control a overhead light in a room based on the position of two light switches. Because the switches are at two different entrances to the room, either switch should be able to change the state (off/on) of the light independently. If both switches are in the “down” position (represented by a zero), the light must be off (represented by a zero). No matter what position the switches are in or the current state of the light, flipping either switch must change the state of the light.

(a) Complete the truth table for the circuit:

S_0	S_1	L
down (0)	down (0)	off (0)
down (0)	up (1)	
up (1)	down (0)	
up (1)	up (1)	

(b) Create a gate-level circuit (using and, or, not, nor, nand) for the logic function:

(c) What is the common name for this function?

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6. [1 Point] **Last and Most Important Question!** Give us your feedback.

(a) How many hours did you spend on this assignment?

(b) On a scale of 1-5, how difficult did you find this assignment? (1-easiest, 5-most difficult)

(c) Do you have any other comments on your experience completing this assignment? What are they?